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A Modification in Euclidean Distance Calculator Circuit with the Aim of English-Numeral Recognition

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***Abstract* — In this brief, a current-mode Euclidean distance calculator circuit which acts as a numeral recognizer is proposed. This recognizer circuit consists of three sub-circuits: a subtracter-rectifier circuit, a squarer/divider circuit, and a geometric-mean circuit. This recognizer can be easily extended for other applications with more input dimensions such as character recognition. Designed circuits were simulated using HSPICE by level 49 parameters in 0.35µm standard CMOS technology. Simulation results have shown better accuracy and lower power in comparison with the previous works.**

***Keywords* — Euclidean distance, Geometric-mean circuit, squarer/divider circuit, translinear loop.**

I. INTRODUCTION

The purpose of recognition is to specify an unknown input to a category with similar characteristics. It plays a significant role in various fields of applied science, e.g., pattern recognition, artificial intelligence, and statistics [2-4].

We can implement a recognizer in three ways: digital, analog or a combination of both methods. Analog implementation of classification/recognition algorithm has a series of advantages over other implementations. In analog implementation we are facing less complexity in comparison with digital counterpart, also, A/D and D/A interfaces are useless. Furthermore, the use of analog circuits for performing parallel processing can increase the efficiency specially the velocity of signal processing. Euclidean distance calculator is an interesting method to implement classification algorithm [8]. Several researchers have worked on designing of Euclidean distance calculator circuits with the purpose of recognition, to guess the right category for each input pattern. Seevinck proposed a bipolar vector summation circuit in voltage-mode approach. however, for the aim of extension, a specific current source must be adjusted [9]. Landolt proposed an Euclidean distance computing circuit with MOS technology but for extending each dimension some adjustment is necessary, which is a disadvantage since it causes some difficulties [10]. Liu and Chang implement their circuits in MOS technology in voltage-mode approach, as a result the supply voltage level reduction has a clear impact on the dynamic range of the circuits [11].
Since current-mode approach enables us to use a wide dynamic range with small voltage swings, it is considered as our processing variables. Some current-mode Euclidean distance calculator circuits were also proposed to get the mentioned benefits from the current mode approach [5-7].
In this brief, a recognizer circuit is proposed. This recognizer is based on the concept of the Euclidean distance calculator. This construction composed of four sub-circuits: the current-mode subtracter- rectifier circuit proposed by Liu *et al*, the squarer/divider circuit, and the geometric-mean circuit proposed by Lopez-Martin *et al.* [12-18]. It is worthwhile to mention that all the transistors are biased in the saturation region instead of in the sub-threshold region to achieve a better signal-to-noise ratio (SNR), higher speed and the more important is to overcome the mismatch of the devices. More features of these circuits are low supply voltage, low power consumption and high dynamic range. Beside, this recognizer can work with gray-level patterns without any additional part and this is due to analog method that we used.

II. CIRCUIT DESCRIPTION

First we will describe the procedure of calculating Euclidean distance and the method of recognizing, then we represent the schematic diagram of related circuits.

The similarity between an unknown input feature pattern $\vec{u}$ and a set of class prototype patterns $\vec{v}_j\,(j=1,...,c)$ is measured by calculating the Euclidean distance $D(\vec{u},\vec{v}_j)$ and classified into one of these c classes according to the least distance that $\vec{u}$ has from one of those classes. See the following steps to realize this method.

Step 1: Input the feature vector $\vec{u}$ to be classified.

Step 2: Compute the Euclidean distance $D(\vec{u},\vec{v}_j)$ between $\vec{u}$ and each class prototype $\vec{v}_j$ by

$$D(\vec{u},\vec{v}_j)=\sqrt{(\vec{u}-\vec{v}_j)\cdot(\vec{u}-\vec{v}_j)}$$
$$=\sqrt{(u_1-v_{j1})^2+...+(u_n-v_{jn})^2} \qquad (1)$$

Since we want to implement our circuits in current mode, we replaced the variables with current signals, the recognizing procedure by an Euclidean distance calculator can be realized as in Fig. 1.

A. Subtracter-rectifier Circuit

This circuit is obviously consists of two parts: a subtracter followed by a rectifier as shown in Fig.2 in which the relationship between input/output can be expressed as follows:

$$I_x = |I_u - I_v| \qquad (2)$$

where I_u and I_v stand for the input current signals while I_x is the resultant output current signal.

We need a rectifier to have the unipolar current signal I_x. The rectifier works based on the core part consists of M_7, M_8 and M_9. By biasing the gate of M_9 appropriately, the core part will take the absolute value of its input. An external voltage source is used to apply

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voltage to V_b . When $I_u - I_v$ becomes negative, the source-to-gate voltage V_{SG7} will be increased and M_7 will be turned on. As a result, $V_{SG9} = V_{DD} - V_{SG7} - V_b$ will be less than the absolute value of the threshold voltage V_{tp}, and M_9 will be turned off. At this time, the input current will be guided into this circuit via the current mirror formed by M_7 and M_8 and transmitted to the output via the nMOS current mirror formed by M_{10} and M_{11}, and the pMOS current mirror formed by M_{12} and M_{13}. Obviously, the input/output relationship can be written as

$$I_x = -(I_u - I_v) \text{ for } (I_u - I_v) < 0 \qquad (3)$$

On the other hand, when $I_u - I_v$ is positive, no current will flow through M_7. In this situation, V_{SG7} is zero, and $V_{SG9} = V_{DD} - V_{SG7} - V_b$ is greater than the absolute value of the threshold voltage V_{tp}. Therefore, the positive current $I_u - I_v$ will be drawn by M_9 and M_{10}, and will be mirrored out via M_{11}. After changing the direction of current via the pMOS current mirror formed by M_{12} and M_{13}, the input/output relationship can be expressed as

$$I_x = I_u - I_v \text{ for } (I_u - I_v) > 0 \qquad (4)$$

Combining (3) and (4) will obtain (2), which confirms the function of a subtracter-rectifier circuit.

B. Geometric-mean circuit

Fig.3 shows the schematics of the Geometric-mean circuit, which is based on the well known trans-linear principle [19]. This is the same circuit were published in [20] with a little difference, that is we used cascade current mirrors to have more accuracy. Knowing that the devices are perfectly matched having long channel length (neglecting channel length modulation (λ=0)):, and the drain current of a MOS transistor in A KVL on the shown loop gives:

$$V_{GS1} + V_{GS3} = V_{GS2} + V_{GS4} \qquad (5)$$

saturation region has the following relation to its gate-source voltage:

$$I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) \qquad (6)$$

Equation (5) can be written as:

$$\sqrt{I_1} + \sqrt{I_3} = \sqrt{I_2} + \sqrt{I_4} \qquad (7)$$

And then

$$I_2 + I_4 = I_{out} + \frac{I_H + I_y}{2} \qquad (8)$$

Since the NMOS current mirrors force I_2 be equal to I_4, the output current will be:

$$I_{out} = \sqrt{I_H I_y} \qquad (9)$$

C. Squarer/divider circuit

In fact the SQ/DIV circuit is the Geometric-mean circuit while the output is replaced by one of the inputs. The designed circuit is shown in Fig.4 According to (9), the output is equal to:

$$I_{x^2} = \frac{I_x^2}{I_H} \qquad (10)$$

D. Euclidean Distance Calculator Circuit

We can describe an Euclidean distance calculator as below with regards to the three basic circuits mentioned above [16]. According to Fig.1 the input current signals I_{u_i} and $I_{v_{ji}}$ applied to the i_{th} subtracter-rectifier circuit obtains the unipolar current signal

$$I_{x_{ji}} = \left| I_{u_i} - I_{v_{ji}} \right| \qquad (11)$$

Then guiding the unipolar current signal $I_{x_{ji}}$ and the constant current signal I_H to the squarer/divider circuit yields

$$I_{x_{ji}^2} = \frac{I_{x_{ji}}^2}{I_H} \qquad (12)$$

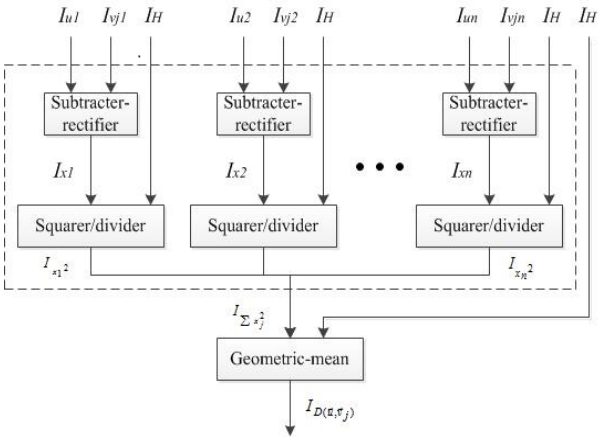

Fig.1. Block diagram of the proposed recognizer

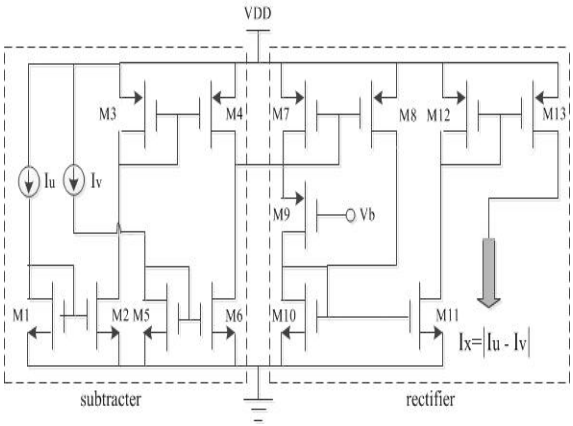

Fig.2. Schematic of the subtracter-rectifier circuit

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Next connecting all the output currents $I_{x_{ji}^2}$ of these squarer/divider circuit together acquires

$$I_{\sum x_j^2} = \sum_{i=1}^{n} \frac{I_{x_{ji}}^2}{I_H} \quad (13)$$

Finally, applying $I_{\sum x_j^2}$ and the constant current signal I_H to the geometric-mean circuit realizes the Euclidean distance circuit with the input/output relationship expressed as

$$I_{D(\vec{u},\vec{v}_j)} = \sqrt{I_{\sum x_j^2} I_H} = \sqrt{\sum_{i=1}^{n} \frac{I_{x_{ji}}^2}{I_H}} \quad (14)$$
$$= \sqrt{(I_{u_1} - I_{v_{j1}})^2 + \ldots + (I_{u_n} - I_{v_{jn}})^2}$$

where

$I_{D(\vec{u},\vec{v}_j)}$ current domain representations of the Euclidean distance $D(\vec{u},\vec{v}_j)$;

I_{u_i} current domain representations of the Euclidean distance *i*th entry of $\vec{u}$;

$I_{v_{ji}}$ current domain representations of the Euclidean distance *i*th entry of $\vec{v}_j$.

Obviously, the dimension of input variables can be easily extended in a really simple way by adding all the subcircuits except the geometric-mean in parallel, provided that the total current injecting to the input terminal of the geometric-mean does not exceed its dynamic range[1].

III. Experimental Results

The current-mode recognizer circuit based on the block diagram of Fig.1, and the proposed G-mean circuit of Fig.3 was designed. The circuit was simulated by HSPICE with TSMC 0.35 um CMOS technology, I_H=10uA, *V*dd=*3.3*V and V_b *=1.5V* were applied. Furthermore, to prevent the body effect in the transistors, their source and substrate must be tied together.

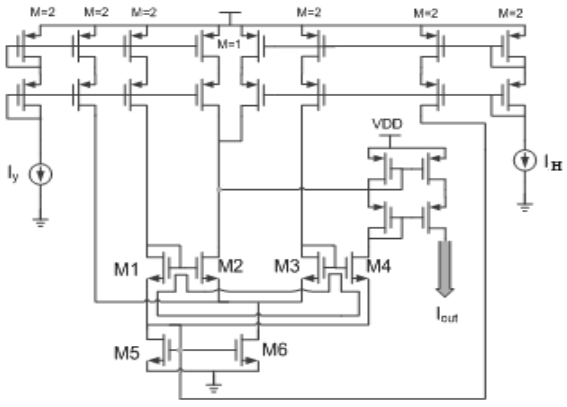

Fig.3. Geometric-mean circuit

To illustrate the function of this circuit, we have used English-numeral patterns Fig.5 For simplicity, each English-numeral pattern (1,2,…,0) is demonstrated by a grid. Each pixel of the grid is fulfilled with either white or black colour and valued by 0μA/5μA current signal. The class prototype patterns indicated with $\vec{v}_j$,and the input patterns that we want to classify indicated with $\vec{u}$. The test equipment for English-numeral pattern recognition is represented in Fig.6. The Euclidean distance between each input pattern and the ten prototype patterns is measured.

During simulation, the set of each input pattern was assumed constant while the 10 prototype patterns were sequentially called, beginning from pattern *V*1 to pattern *V*10 (Fig.6), calling the next prototype pattern every 1us. Under these conditions, the corresponding output of the input patterns of *U*1, *U*2 … *U*10 are shown in Fig.7, respectively. Obviously, the least of this distance suggests the nearest match between input pattern and prototype patterns.

Fig.7 shows the empirical results of this recognizer dealing with English-numeral patterns. It shows the similarity of each input pattern at each time to the each prototype pattern. The results of simulation illustrate that these prototype patterns with the maximum matching degree of the input patterns *U*1, *U*2, …, *U*10 are *V*1, *V*2, …, *V*10 at the times 1 us, 2 us, …, 10 us, respectively. These profiles indicates that this circuit can recognized input patterns correctly.

To assess the speed of the recognizer circuit, first we define the identification time. It is the time required for recognizing a pattern in the circuit and will be evaluated by maximum rise time/fall time of the calculator circuit [3]. The identification time for our circuit is about 150ns.

IV. Conclusion

In this brief, a current-mode recognizer circuit has been proposed. This circuit is designed based on the current-mode subtracter-rectifier circuit, the squarer/divider circuit, and the geometric-mean circuit. Besides the functional testing, its transient response and power consumption were also measured.

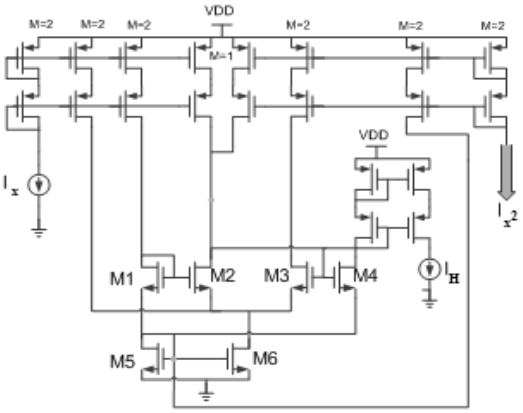

Fig.4. Squarer/divider circuit

The current-mode approach of the circuit allows it to operate at 3.3V supply voltage with 11mW power consumption. Table I shows a comparison between our work and previous Euclidean distance calculator. Relying on the parallel processing characteristic and the mentioned merits, this circuit is suited to real-world low-power and low supply voltage applications.

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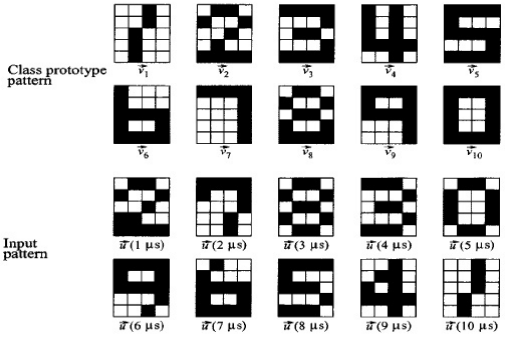

Fig.5. Class prototype pattern $\vec{v}_j$ and input patterns $\vec{u}$ for English-numeral recognition

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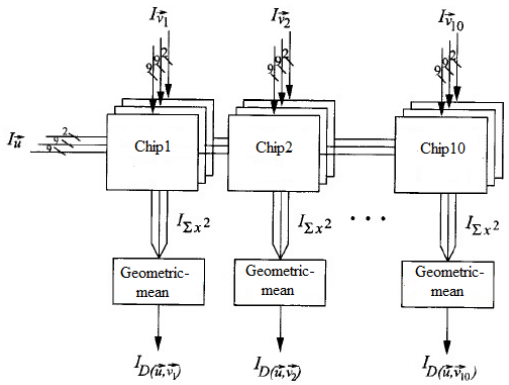

Fig.6. Test fixture for English-numeral recognition

TABLE I. A comparison with previous works

Parameter	Ref. [1,16]	Ref. [5]	Ref. [6]	This Work
Technology	0.6u	0.35u	0.5u	0.35u
Supply Voltage	3.3V	3.3V	3.3V	3.3V
Power Consumption	15mW	Expected >10mW	16mW	11mW

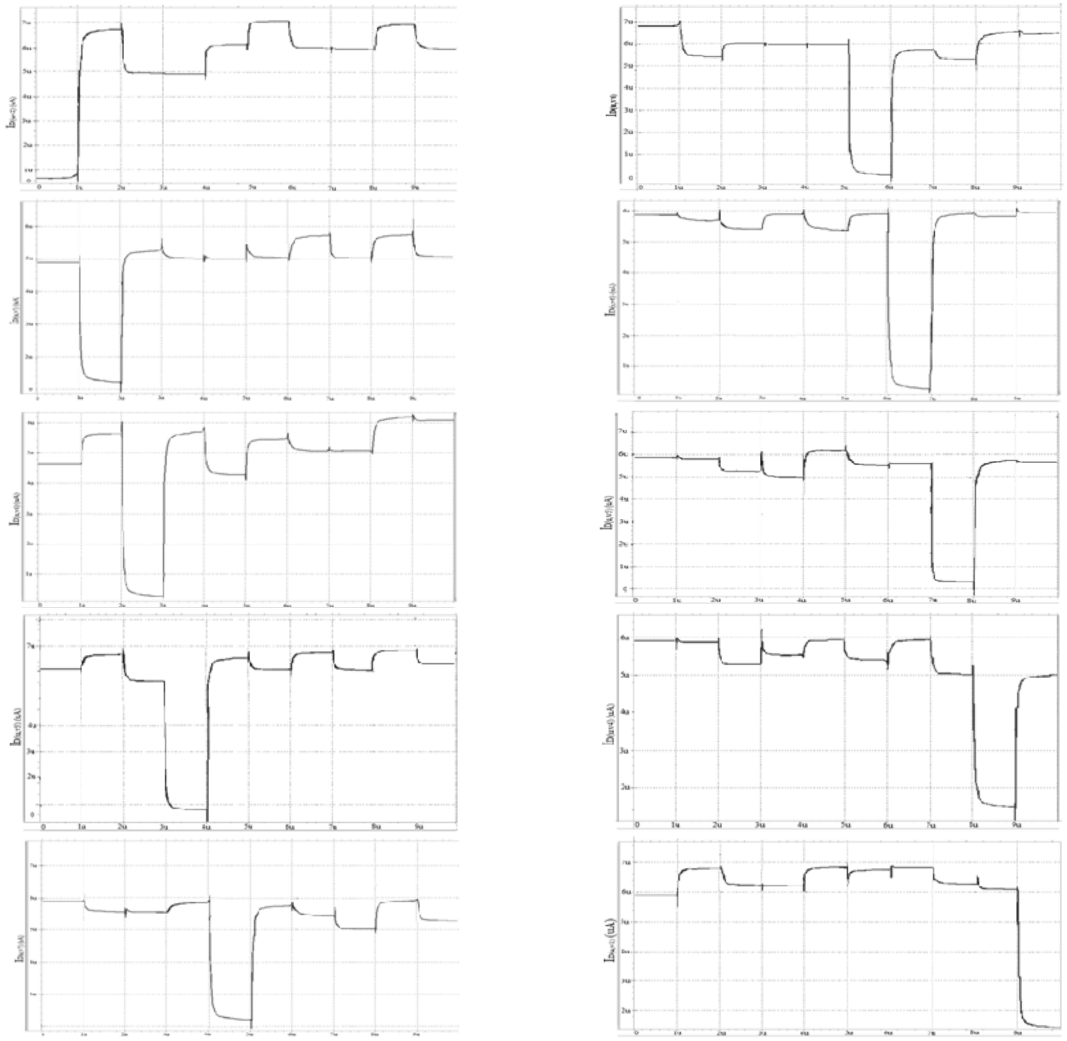

Fig.7. Experimental results of Euclidean distance calculator circuit for English-numeral recognition