International Journal of Electronics Communication and Computer Engineering
Volume 3, Issue 5, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

Modified XY Routing Algorithm with Scheduler for NOC

Shubhangi D. Chawade **Mahendra A. Gaikwad** **Rajendra M. Patrikar**

Abstract - **Network on Chip (NoC) is a new prototype to formulate the interconnections in a System on Chip (SoC). With encroachments in Noc technology the bus structure has been replaced with an integrated network that results in no traffic congestion. Today a NoC consist of devices that use the network routers directing traffic among devices and wire analogous to the Internet. Thus efficient network topology and routing algorithm are imperative to the NoC design. This paper presents a modified XY routing algorithm combined with a scheduler to be used on NoCs. The proposed method is a fast way to transferring data via a specific path between two nodes in the network and the scheduler in proposed method voids collision.**

Keywords - **Routing Algorithms, Networks on Chip (NoC), XY Routing Algorithm, Packet Switching.**

I. INTRODUCTION

The advancement in the semiconductor technology in the last few decades has led to seemingly endless miniaturization of electronic components. This has enabled designers to build sophisticated computing structures on silicon chips. Earlier what used to be a system of discrete chips has today become a single chip system, thus the SoC concept was born. Earlier buses were the mostly used interconnection between components, but with today's increasing complexity buses have several limitations that make them not fit the today's SoC requirements.

Since the old bus technology can not fit the communication requirements of the future SoCs, new methods have been developed since 1999. One of the best methods to solve the bus problem is called Network on Chip (NoC). Network on Chip (NoC) is slowly being accepted as an important paradigm for implementing communication among various cores in a SoC [1]. In last few years NoC has received more and more attentions from both the academic researches and the industrial development. So far, several different NoCs have been developed.

Fig 1 shows the conceptual view of a NOC where, each tile is composed of a resource(R) and a switch or router(S). The router is connected to the four neighboring tiles and its local resource via channels. Each channel consists of two directional point-to-point links between two routers or a router and a local resource [4].

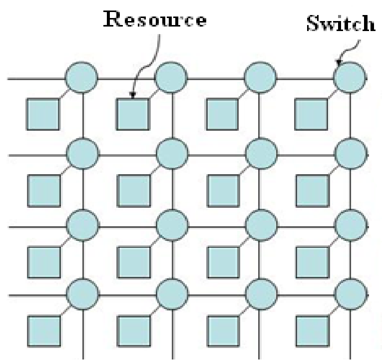


Fig.1. Structure of 4x4 NOC

There are a couple of performance requirements that every Network on Chip implementation must satisfy:

- Small latency,
- Guaranteed throughput,
- Path diversity,
- Sufficient transfer capacity
- Low power consumption.
- Fault and distraction tolerance &
- Architectural requirements of scalability and programmability.

The network traffic in NoC network is classified into two types as:

- Guaranteed Throughput (GT) Traffic
- Best Effort (BE) Traffic

Guaranteed Throughput (GT) also sometimes referred to as Guaranteed Service (GS) works superlatively well with circuit switched network type routing algorithms, where the GT supplier assumes that the sender complies with networks operation requirements [5].

Best-effort network traffic as the name suggests makes the best effort to route the packets to the destination but there is no guaranty of packet delivery. Since BE is not concerned with delivery of the packet it uses less overheads as compared to GT above. In such cases latencies can be more variable and in the worst situations packets can be lost [6].

II. NOC ROUTING BASICS

In networks on chip (NoC), routing is done to connect different components together in the most efficient manner. For example selecting a short path may be important in one situation, while creating an appropriate traffic load balancing may of greater importance in other situation. A vast number of routing algorithms have been proposed and all of them have some pros and cons compared to each other. Thus one routing algorithm can be advantageous in one NoC while the same can be not of much worth in other NoC. These algorithms are often classified in two groups

[3] that is Deterministic algorithms and Adaptive algorithms.

The deterministic algorithms usually have less computation and are able to find the next hop in a shorter time. The deterministic algorithms are mostly based on indexes and therefore are more suitable in NOCs which have predetermined structures. These algorithms are used in both regular and irregular networks. Because of the simplified logic, the deterministic routing provides low routing latency and good reliability when the network is not congested. These algorithms suffer from low tolerance against the possible faults in the networks and thus as the packet injection rate increases, they provide throughput and efficiency degradation as they cannot dynamically respond to network congestion.

On the other hand adaptive algorithms often need more computations and in order to select the correct path they need some information about the current state of the network. The adaptive algorithms simultaneously perform the routing and packet forwarding. After each hop they select the next hop according to the current state of the nodes and links traffic. Thus there is always a possibility of live lock occurrence in them [6, 7].

Deadlock, livelock and starvation are the most potential problems on both oblivious and adaptive routing.

III. XY Routing

Wang Zhang and Ligang Hou [8] proposed Classic XY (Static XY OR XY) routing algorithm which is one of the type of Dimension order routing (DOR) which is a typically a minimal turn algorithm and is more suitable for networks using mesh or torus topology. XY routing algorithm routes packets first in x-direction (or horizontal direction) to the correct column and then in y- direction (or vertical direction) to the receiver. In XY routing the addresses of the routers are their xy-coordinates. As in figure 2 a packet will be routed to the correct horizontal position first from the source node and then will be routed to the correct vertical position to reach to the destination node. Considering the example of a 4x4 NoC as in figure 2 and a node (2,1) wants to send a packet to node (4,4), then the packet is first routed horizontally 4 nodes and then down vertically 3 nodes to reach the destination node. XY routing produces minimal paths without redundancy and one of the advantages of XY routing is that it never runs into deadlock since it is impossible for a cyclic channel dependency to arise if channels are acquired XY order [9], as shown in figure 3.

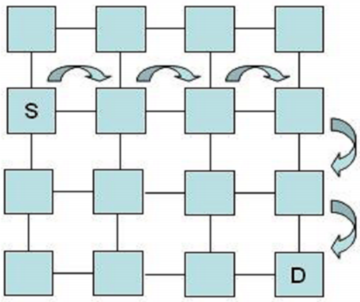


Fig.2. XY routing from router S to router D in 4x4 NOC

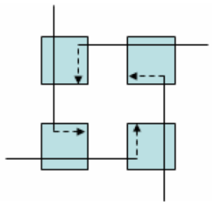


Fig.3. Deadlock is not possible with X-Y routing

However despite the advantages of simplified calculation and removal of deadlock or livelock problem, there are some problems in the traditional XY routing. One important issue with traditional XY routing algorithm is that the algorithm causes the biggest load in the middle of the network which does not extend the traffic regularly over the whole network. Thus there is a need for algorithms which equalize the traffic load over the whole network and are yet simple and efficient.

An extension to the XY-routing algorithm is called S-XY (Surrounding XY). Since it is an extension it inherits the properties of local-decisive and deadlock free of XY-routing algorithm. The routers in Surrounding XY routing (S-XY) has three different routing modes:

- N-XY (Normal XY) mode: The routers here work as a normal XY router. A packet is first sent horizontally to the target column and then vertically to the target row. Routing stays on NXY mode as long as network is not blocked and routing does not meet inactive routers.
- SH-XY (Surround horizontal XY) mode: The router enters this mode, when its left neighbor or its right neighbor (horizontal neighbor) is deactivated SV-XY (Surround vertical XY) mode: The router enters this mode, when its upper or lower neighbor is inactive.

The routers in the SH-XY and SV-XY modes add a small identifier to the packets that informs the other routers that these packets are routed using SH-XY or SV-XY mode and hence other routers do not send these packets backwards. In SH-XY/SV-XY modes routes packets to the correct column/row on the basis of coordinates of the destination bypassing the packets around the inactive routers along the shortest possible path. This condition is a bit different in the SV-XY mode since the packets are already in the right column. Packets can be routed to left or right i.e., in the correct row. Q-routing, XY-routing and Surrounding XY routing is most commonly used in a DyNoC (Dynamic Network on Chip).

International Journal of Electronics Communication and Computer Engineering
Volume 3, Issue 5, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

IV. Proposed Method Modified XY Routing

The proposed method uses a modified XY routing algorithm combined with a scheduler to be used on NoCs. The proposed method uses the 48 bit packet format to route any packet across the NoC.

0	1	2	3	4 – 35	36 – 41	42 – 47
X	X	X	Req (1)	Data (32)	Destn Addr (6)	Src Addr (6)

Fig.4. Packet Format

First three bits are don't care, request bit is initially set to '0' and is used by the scheduler. The last 6 bits are the source address and the bits from 36 to 41 are the destination address. Consider that 3 nodes want to send the packet to some destination. The scheduler in this case will set the Req bit for these nodes to '1' and will further schedule these nodes to send data one by one based on first-cum-first basis. Thus packets with Req bit set are only forwarded across the network. The simulation is performed on ModelSim SE PLUS 6.2c Simulator and the considered simulation parameters are as given below:

- The packet size is 48 bits.
- The simulation runs on clock frequency of 8 GHz.
- Synthetic traffic generators generate traffic in the first 2 clock cycles with warm-up period of 1 clock cycles.
- Performance metrics include average latency per bit and average throughput packets per second for each channel.
- Packets are generated at each node according to a Gaussian Traffic distribution pattern is uniform
- Mesh Topology is being used for NoC design. The mesh can be 4x4, 5x5 upto 8X8 depending upon the choice.

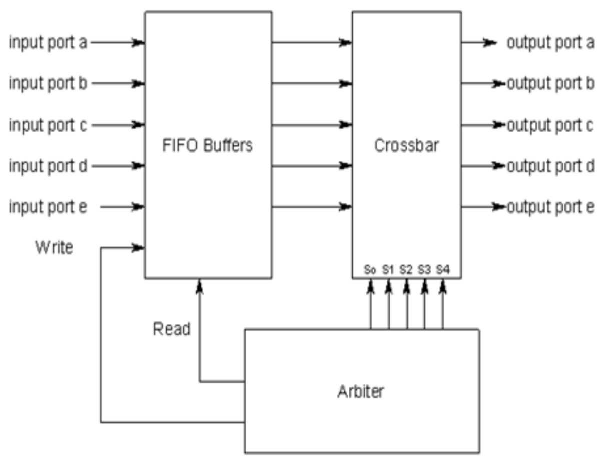


Fig.5. Generic Architecture of On-Chip Router

The heart of an on-chip network is the router, which undertakes crucial task of coordinating the data flow. The router operation revolves around two fundamental regimes: (a) the datapath and (b) the associated control logic. The datapath consist of number of input and output channels to facilitated packet switching and traversal. Fig 5 above shows the design of a implemented router to be used in NOCs. The design of router mainly consists of three parts:

1. FIFO
2. Arbiter
3. Crossbar

Buffering is very essential in NoC for flow control and congestion control. Deciding proper size of buffer is the key issue for getting optimal performance. In this design the buffer of depth four is used to provide input buffering. The length of buffer is equal to the packet size. Since the depth of buffer is four, minimum four clock signals are required for first packet to come out of buffer. Arbiter controls the arbitration of the ports and resolves contention problem. It keeps the updated status of all the ports and knows which ports are free and which ports are communicating with each other. A crossbar switch is an assembly of individual switches between multiple inputs and multiple outputs. The switches are arranged in a matrix. At each crosspoint is a switch; when closed, it connects one of M inputs to one of N outputs. A given crossbar is a single layer, non-blocking switch. The design of crossbar switch has 5 inputs and 5 outputs. According to the select lines generated by arbiter, crossbar establishes the connections between input port and output port.

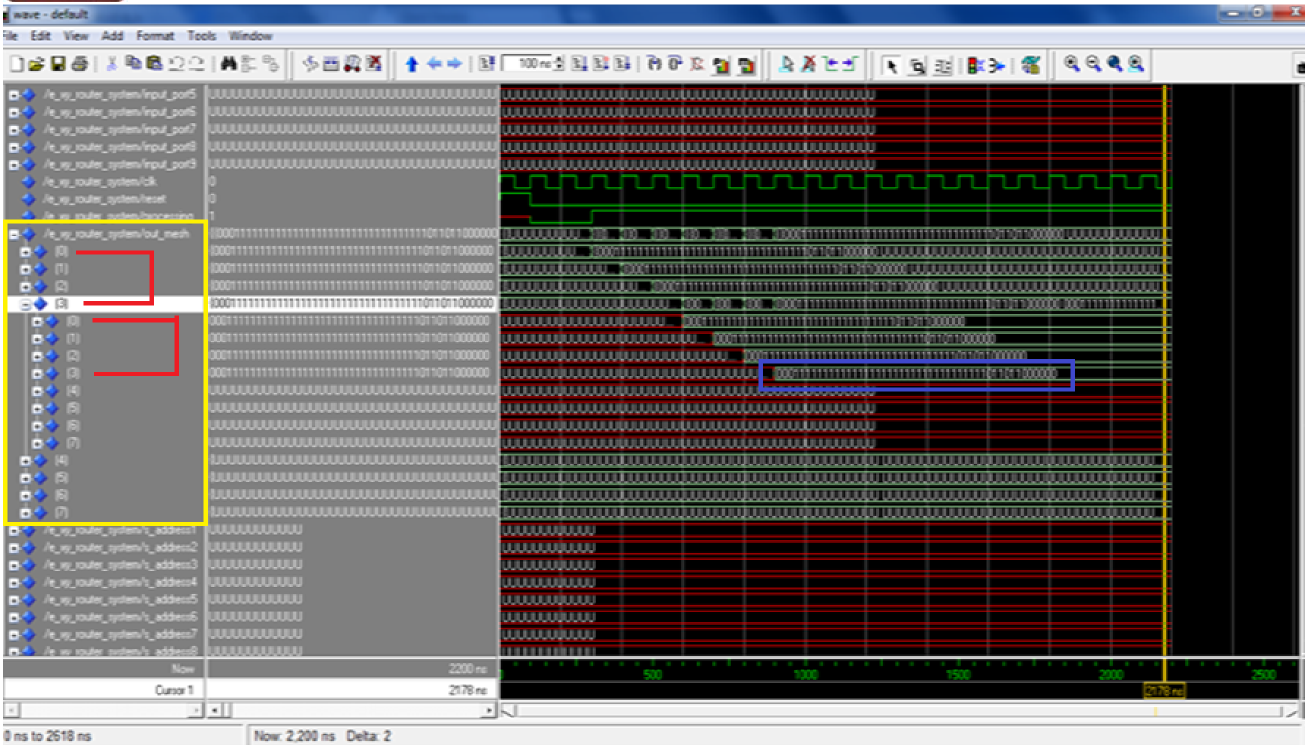


Fig.6. Result of the proposed method

V. Results

Fig 6 shows the output of a node at 0x0 sending the data to a node at 3x3. The packet is first routed along x-direction (marked with red a 1st brace) and the along y-direction (marked with red a 2nd brace). This can be seen from the box highlighted in yellow in fig 6. Box in blue shows the data has reached the destination node at 3x3.
As in table 1 below it can be seen that the latency and throughput is found to be 7.29 per bit and $2.7x10^6$ packet/sec respectively without contention. The extended result is obtains for with and without contention for 3X3 Mesh topology.

Table 1: Results for Contention v/s without Contention

	Without Contention	With Contention
Latency per bit	7.29	7.42
Throughput $x10^6$ packet/sec	2.7	2.2

Table 2: Results for different size of mesh

Mesh size	2X2	3X3	4X4	8X8
Latency per bit	6.77	7.42	7.483	7.5
Throughput $X10^6$ packet/sec	1.2	2.2	3.57	13.7

It shows that more latency and fewer throughputs are calculated in the network. The experiment performed on different size of mesh topology with contention in network.

From Table 2, it is observed that the throughput and latency are directly proportional to mesh size. It can be seen that as the size of the mesh increases the latency and throughput increases.

VI. Conclusions

In this paper, an adequate solution to tackle the main issues associated with the routing in a NoC are addressed. The proposed method presents a modified XY routing algorithm which employs a simple XY routing algorithm combined with a scheduler to be used on NoCs. The results show that the proposed method is a fast and an efficient way to transferring data via a specific path between two nodes in the network and the scheduler further helps to avoid collision. The latency and throughput is found to be 7.29 per bit and $2.7x10^6$ packet/sec respectively for 3X3 mesh topology. The value of latency and throughput increases with increase in mesh size.

References

[1] Kumar, S., Jantsch, A., Soininen, J-P., Forsell, M., Millberg, M., Öberg, J., Tiensyrjä, K., Hemani, A.: A network on chip architecture and design methodology. In IEEE Annual Symposium on VLSI (April 2002).

[2] Liang, J., S. Swaminathan, and R. Tessier, 2000. “aSOC: a scalable, single-chip communication architectures”, In IEEE Int. Conf. on Parallel Architectures and Compilation Techniques, pp: 37.

[3] Rantala, V., T. Lehtonen, J. Plosila, 2006. “Network on Chip Routing Algorithms”, TUCS Technical Report, 779.

[4] J. Henkel, W. Wolf, and S. Chakradhar, "On-chip networks: A scalable, communication-centric embedded system design

[5] Ville Rantala, Teijo Lehtonen and Juha Plosila, "Network on Chip Routing Algorithms", University of Turku, Department of

Information Technology Joukahaisenkatu 3-5 B, 20520 Turku, Finland, TUCS Technical Report, August 2006

[6] K. Goossens, J. Dielissen, A. Radulescu: Æthereal Network on Chip: Concepts, Architectures and Implementations. IEEE Design & Test of Computers, 2005, Volume 22, Issue 5, pages: 414–421.

[7] N. Kavaldjiev, G. J. M. Smit, and P. G. Jansen, "A virtual channel router for on-chip networks," IEEE International SOC Conference, pp. 289-93, USA, 2004.

[8] Wang Zhang, Ligang Hou, Jinhui Wang, Shuqin Geng, Wuchen Wu, Comparison Research between XY and Odd-Even Routing Algorithm of a 2-Dimension 3X3 Mesh Topology Network-on-Chip.

[9] T. T. Ye, L. Benini, and G. De Micheli, "Packetization and routing analysis of on-chip multiprocessor networks," Journal of Systems Architecture, vol. 50, pp.81-104, 2004.

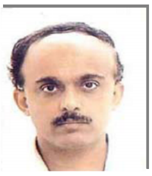
[10] M. Dehyadgari, M. Nickray, A. Afzali-kusha, Z. Navabi: Evaluation of Pseudo Adaptive XY Routing Using an Object OrientedModel for NOC. The 17th International Conference on Microelectronics, 13–15 December 2005.

[11] C. Bobda, A. Ahmadinia, M. Majer, J. Teich, S. Fekete, J. van der Veen: DyNoC: A Dynamic Infrastructure for Communication in Dynamically Reconfigurable Devices. International Conference on Field Programmable Logic and Applications, 24–26 August 2005, pages: 153–158. paradigm," VLSI Design, pp. 845-851, India, 2004.

AUTHOR'S PROFILE

Shubhangi D. Chawade did her BE in Electronics and Telecommunication in 2007 from Nagpur university. She worked as a Lecturer in the department of Electronics Engineering Sevagram (Wardha) and Software Engineer in IBM India Pvt. Ltd.

Dr. Mahendra A. Gaikwad did his BE in Electronics Engineering in 1991 from Nagpur University. He did his MBA in Marketing Management from Nagpur University and he has completed his MCM from Nagpur University. He did his Master's Degree in Personal Administration from Nagpur University. He did his M.Tech in Communication Engineering from Indian Institute of Technology; Bombay in 1998.He was awarded Ph.D. on "Power Optimization in Network-on-Chip architecture" at VNIT, Nagpur. Currently he is working as Dean (R&D), Professor & Head, Department of Computer Engineering at Bapurao Deshmukh College of Engineering, Sewagram (Wardha). He is the life member of professional bodies like Indian Society for Technical Education, Institution of Engineers (India), Indian Society for Telecommunication Engineers. He is also invitee member of Institution of Engineers (India), Nagpur local Chapter, Nagpur. He is the member of Computer Society of India.



Dr. Rajendra Patrikar did his M.Sc. in Physics from Nagpur University. He did M.Tech in Electrical Engineering from IIT Bombay. He joined as Research engineer in the Microelectronics Project at IIT Bombay. He completed his Ph.D. from the same department. He joined as faculty at IIT Bombay after working for a year at Computervision R&D Pune. Later he moved to Singapore to work in TECH Semiconductor in Advance Device Technology. After working there for three years he moved Institute of High Performance Computing Singapore where he carried research work in the area of CAD for VLSI and nano-electronics. He has published about 30 papers International Journals, International Conferences and also filed one patent in USA in the area of VLSI Currently he is working as a Professor & Head, Electronics and Computer Science Department VNIT, Nagpur.