

Design and Implementation of Tied Output Dynamic Dual Clocked Comparator

Priya Patne^{1*} and Sandip Nemade²

^{1,2}Department of Electronics and Communication, TIT, Bhopal (India).

*Corresponding author email id: priya.patne2@gmail.com

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Abstract – Present day technology has completely shifted towards the digital paradigm. However, most of the practical real life signals and data happen to be analog in nature. Hence, the natural need for analog to digital conversion arises. However, how accurate the analog to digital conversion process would be depends on the effectiveness of the comparator circuit of the analog to digital converter circuit. The comparator performs the task of comparing two signals in general. There are several metrics which govern the efficacy of the comparator circuit which are the sampling frequency or speed, power consumption, worst case delay, supply voltage and size. Its always envisaged to design the comparator in such a way that it is compact, fast yet consumes low power. In the proposed work, a dynamic double-clocked comparator circuit is designed and evaluated in terms of the standard performance metrics. It has been shown that the proposed comparator circuit achieves lesser power consumption, size and higher clock frequency compared to conventional dual clocked comparators.

Keywords – Analog to Digital Converter (ADC), Comparator, Double Clocked Comparator, Sampling Frequency, Power Consumption, Worst case delay, Technology Size.

I. INTRODUCTION

Comparator circuits are the basic building block of analog to digital converters. The speed and the efficacy of the analog to digital conversion process is critically controlled by the comparator circuit's operational performance. A comparator can be empirically defined as a circuit which compares two signals.

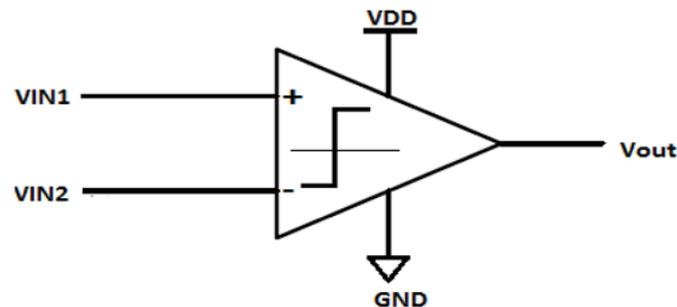


Fig. 1. Empirical Comparator Operation.

The figure above depicts the basic schematic of the basic comparator operation. It can be seen that the comparator has two inputs which are V_{in1} and V_{in2} [1]. The comparator compares the two signals which are considered to be voltage waveforms. The operation can be mathematically understood as:

$$\text{If } V_{in1} > V_{in2}, V_o = V_{DD} \quad (1)$$

$$\text{Else If } V_{in1} < V_{in2}, V_o = gnd \quad (2)$$

Here,

V_{DD} is considered as logic 1

gnd is considered as logic 0.

Often, logic 1 is termed as V_{OH} i.e. High Output Voltage and gnd is termed as V_{OL} i.e. Low Output Voltage.

There always creeps in some uncertainty in when the output makes a transition from high to low or low to high logic levels. Moreover, noise effect can also render inaccuracy to the comparator transfer curve. This situation is depicted below:

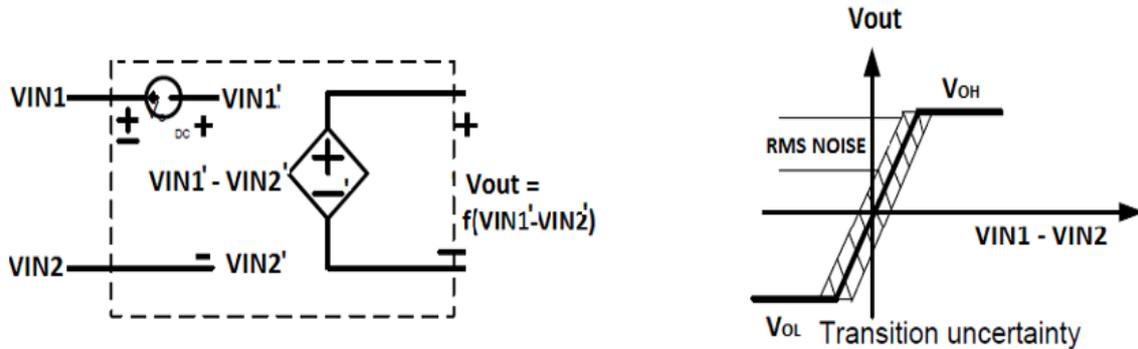


Fig. 2. (a) Small signal voltage equivalent of comparator (b) Transfer curve of the comparator circuit.

A fundamental classification of comparator circuits is given in the figure below based on the operation or functioning.

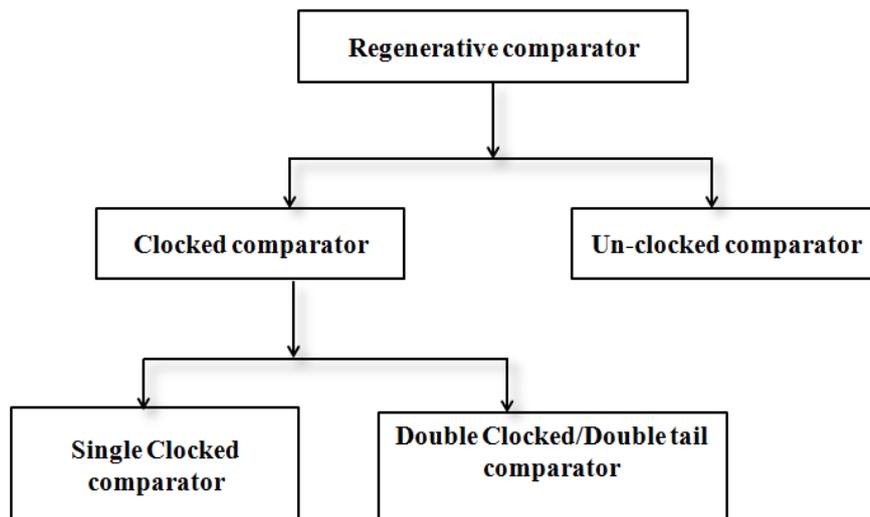


Fig. 3. Classification of Comparators [10].

II. DOUBLE CLOCKED COMPARATORS

Fundamentally, comparators can utilize the supply voltage V_{DD} for the entire time span of operation and hence may not require a clock. This however results in increased power consumption. On the contrary a contrasting approach is to design the comparator in such a way that it utilizes the power from the source V_{DD} only for: [1], [11]

1. High level of the clock.
2. Low level of the clock.
3. Rising edge of the clock or
4. Falling edge of the clock.

In such a case, the comparator saves energy or power. Such a comparator circuit is said to be a clocked comparator. The clocked comparators can again use one or two clocks depending upon the operation of the circuit. This results in the single clocked or double clocked comparator.

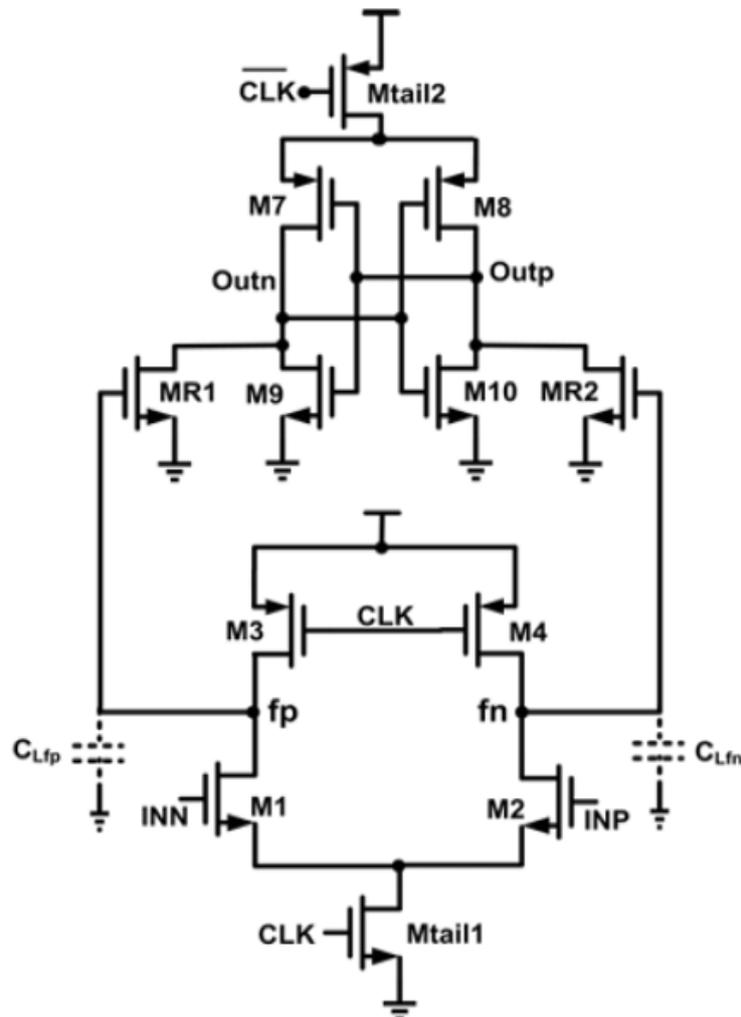


Fig. 3. Basic Double Clocked Comparator.

Figure 3 depicts the basic double clocked comparator with two inputs IN_P and IN_N . The comparator also has two outputs Out_P and Out_N . The circuit can be designed to start working either at the rising edge or the falling edge of the clock pulse. The rate of change of the voltage decay of the inputs governs the output of the comparator i.e. the gradient (g) governs the final output [7]

$$g = \frac{dv}{dt} \quad (3)$$

Here,

V represents the input voltages.

t represents the time.

III. PROPOSED DOUBLE CLOCKED COMPARATOR WITH TIED OUTPUTS

The proposed double clocked comparator is designed to improve upon the sampling speed and the power consumption of the circuit.

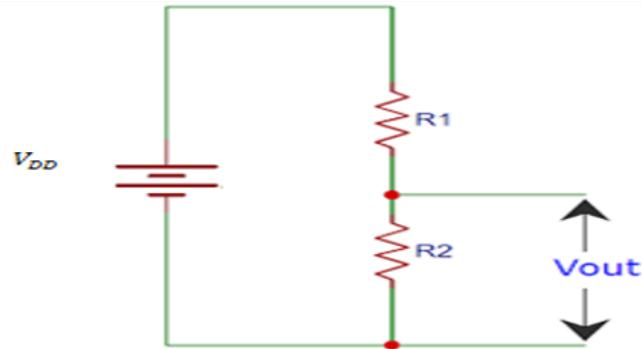


Fig. 4. The Voltage Divider Circuit.

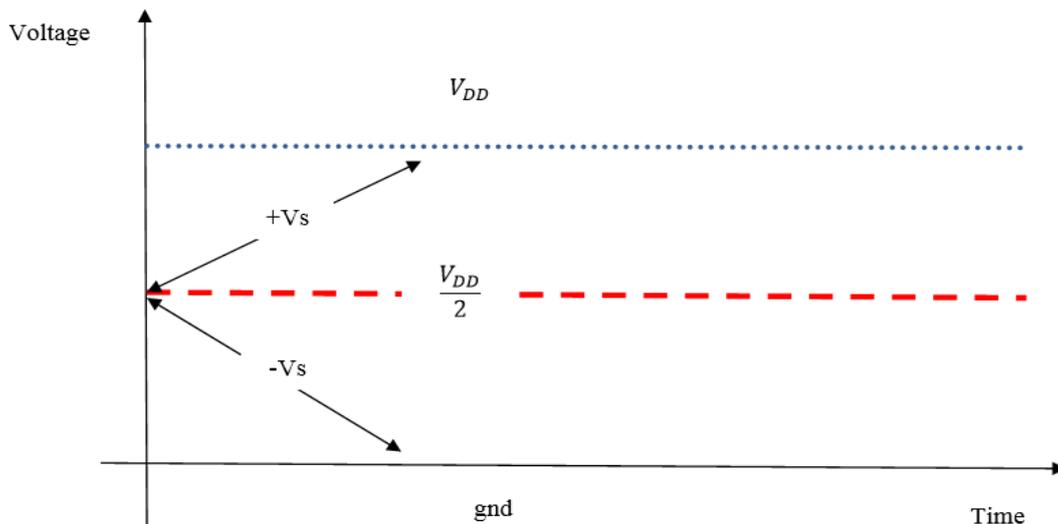


Fig. 5. Voltage Swing of Output with proposed approach.

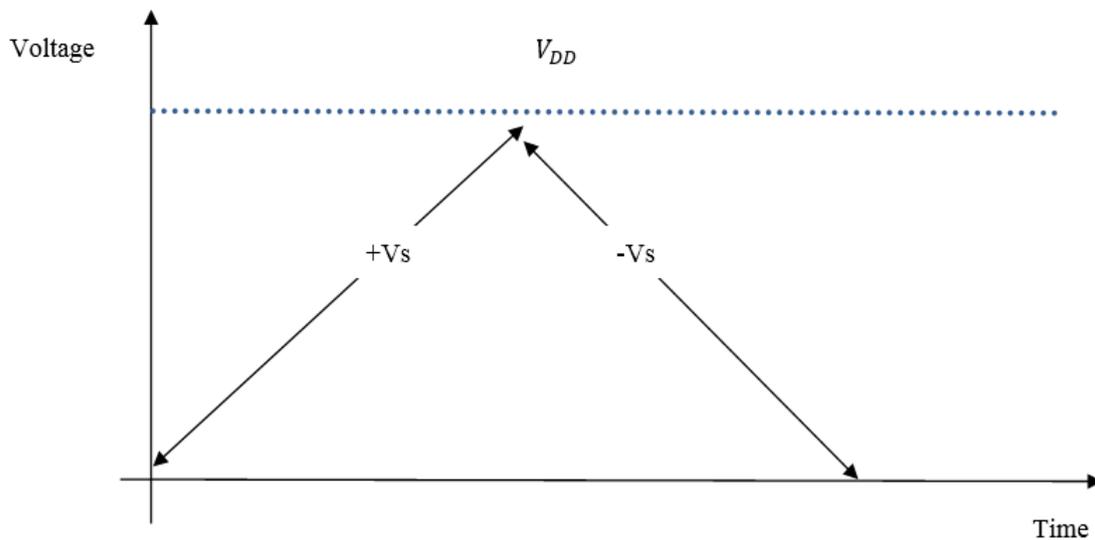


Fig. 6. Voltage Swing with Conventional Approach.

Here,

V_{DD} represents supply voltage.

gnd represents ground.

V_s represents voltage swing.

It can be clearly seen that the voltage swing reduces from V_{DD} to $V_{DD}/2$ thereby considerably reducing the time the output voltage needs to travel before each conversion.

The output voltage across R_2 is given by:

$$V_{out} = \frac{R_2}{R_1+R_2} V_{DD} \tag{4}$$

If the terminals $Outp$ and $Outn$ (one of which is at V_{DD} and the other is at gnd), are shorted, then assuming the bulk resistance of the shorting transistor to be acting equally at both terminals, the output voltage boils down to:

$$V_{out} = \frac{R}{R+R} V_{DD} = \frac{V_{DD}}{2} \tag{5}$$

Thus in the beginning of every conversion, the outputs start at $\frac{V_{DD}}{2}$ in place of V_{DD}

But this phenomenon of pulling up and pulling down doesn't need both the transistors to reach a common **Zero Voltage Level** rather it begins the reset state as soon as both transistors reach a **Common Voltage Level**. As it can be inferred or even seen from Fig.4.3 that it takes lesser time for both the transistors to reach a common voltage level as they don't need to traverse the **Entire Dynamic Range** between the high and low voltage levels. This effect considerably reduces the sampling time thereby bringing about a substantial change in the **Maximum Sampling Frequency**. It holds common ground of $\frac{V_{DD}}{2}$. Thus, clearly the comparators output reaches to V_{DD} or 0 V depending upon the position of the output voltages.

V. RESULTS

The proposed comparator comparing with the conventional double-tail dynamic comparators circuit has been simulated in a 90nm CMOS technology using Cadence with $V_{DD} = 1.2V$. The circuit of proposed comparator is implemented Cadence. The input parameters are given below:

Table 1. Comparator Parameters.

S. No	Input parameters	Value
1	Supply voltage	1 V
2	Clock Voltage Range	0V – 1.2V
3	Clock Frequency	3.3 GHz
7	Clock Pulse Width	1ns
8	Pulse period	0.3ns
9	Input Voltage swing	0.0mV – 2.0mV
9	Reference Voltage	1mV

The proposed dynamic double clocked comparator is simulated with the help of Cadence and observed the output of comparator. **CMOS Technology and W/L Ratio:** The technology used here is 90nm which is considerably less compared to the common earlier technology scale of 180nm. The value of β , i.e. W/L is 4:3. The results obtained from the model of the proposed comparator can be summarised and explained under the following heads individually, for which the table tabulating the final results has been referred: The evaluation parameters are:

1. Maximum sampling frequency.
2. Power consumption or energy per conversion.
3. Supply Voltage.
4. Worst Case delay.
5. Technology size.

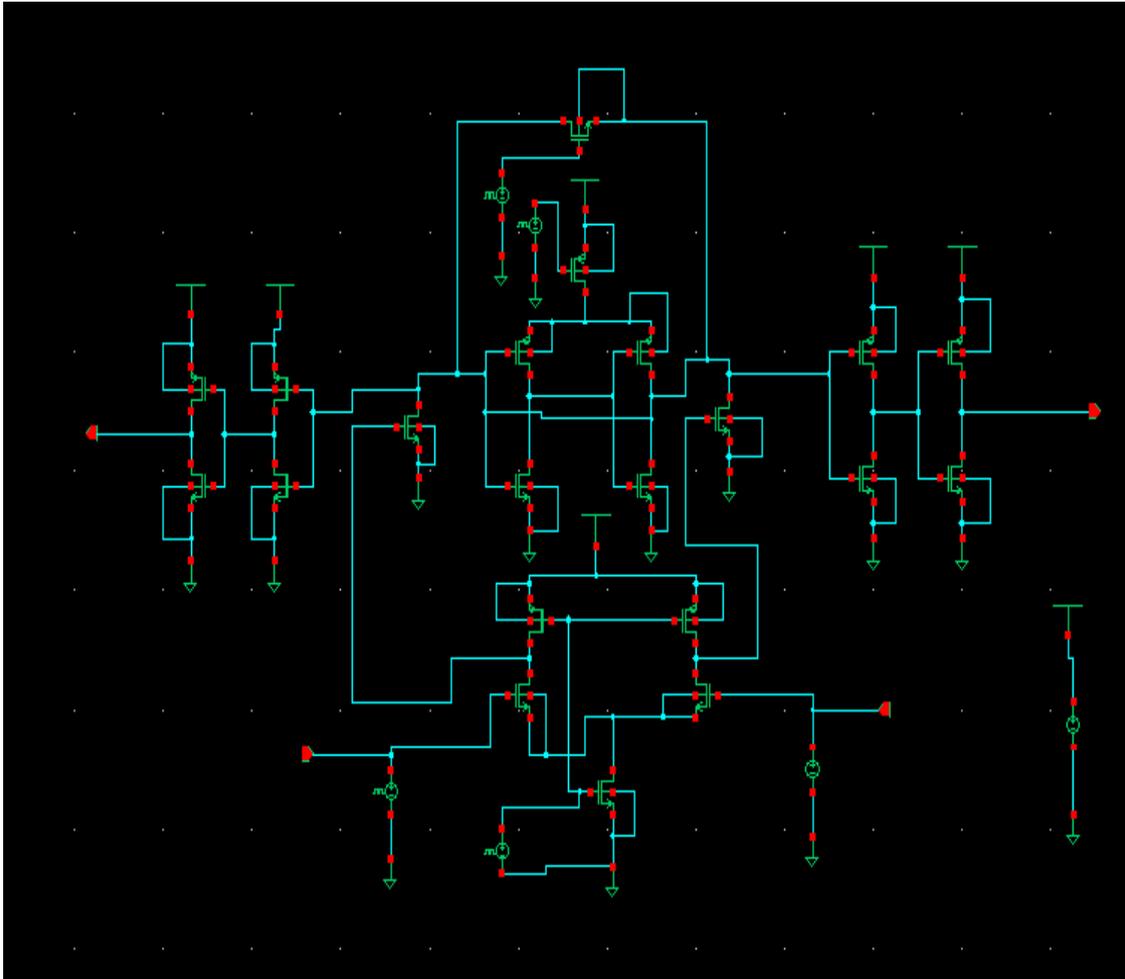


Fig. 7. Proposed Double tail Comparator circuit design in Cadence.

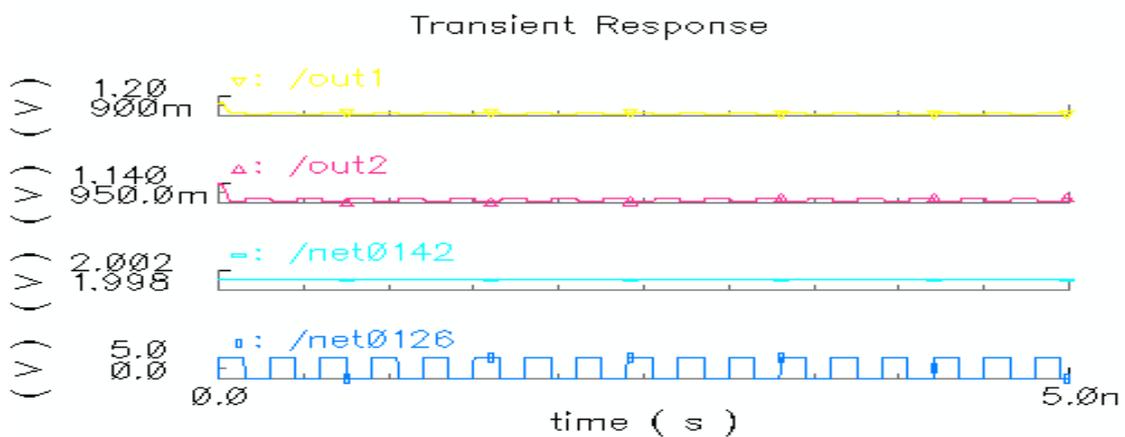


Fig. 8. Output of Proposed Double tail Comparator circuit at clock frequency 3.3 GHz.

It can be clearly seen that the voltage swing reduces from V_{dd} to $V_{dd}/2$ thereby considerably reducing the time the output voltage needs to travel before each conversion.

Clock pulse time period = 0.325ns

The clock frequency of the proposed comparator can be calculated by the given relation

$$\text{Maximum clock frequency} = \frac{1}{\text{Clock pulse time period}} \text{Hz} \tag{6}$$

$$\text{Maximum sampling frequency} = \frac{1}{0.3 \times 10^{-9}} \text{Hz} \tag{7}$$

Maximum sampling frequency $\approx 3.33 \times 10^9$ Hz

Another important parameter which is critical for the comparator design is the power consumption. It should however noted that the absolute power consumption in this case is immaterial. The reason being the fact that if the comparator circuit works for a longer time, then the overall power consumption will increase.

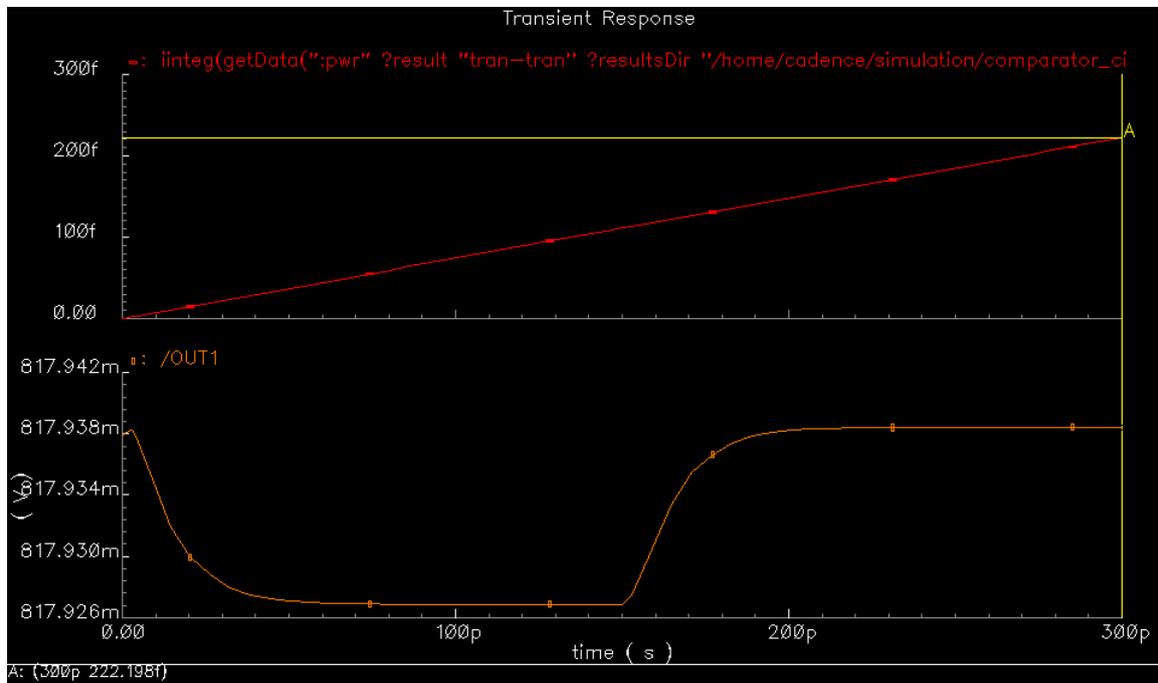


Fig. 9. Transient output for Energy per Conversion.

Mathematically,

$$P_{TOT} = f(t) \tag{8}$$

Here,

P_{TOT} is the total power consumption

f represents a function of

t represents time

Hence, the apt way to measure the power consumption of a comparator circuit is by measuring the power for one clock cycle i.e. energy per consumption. This can be computed by computing the area under curve of Power-time curve. Mathematically, energy per conversion is given by:

$$E_{pc} = \int_0^T p(t)dt \quad (9)$$

Here,

E_{pc} is the energy per conversion

$p(t)$ is the power as a function of time

t is the time metric

From the figure, it can be seen that the energy per conversion for one clock cycle i.e. 0.3ns or 300 fs is 222.198 fJ i.e. 0.222198pJ.

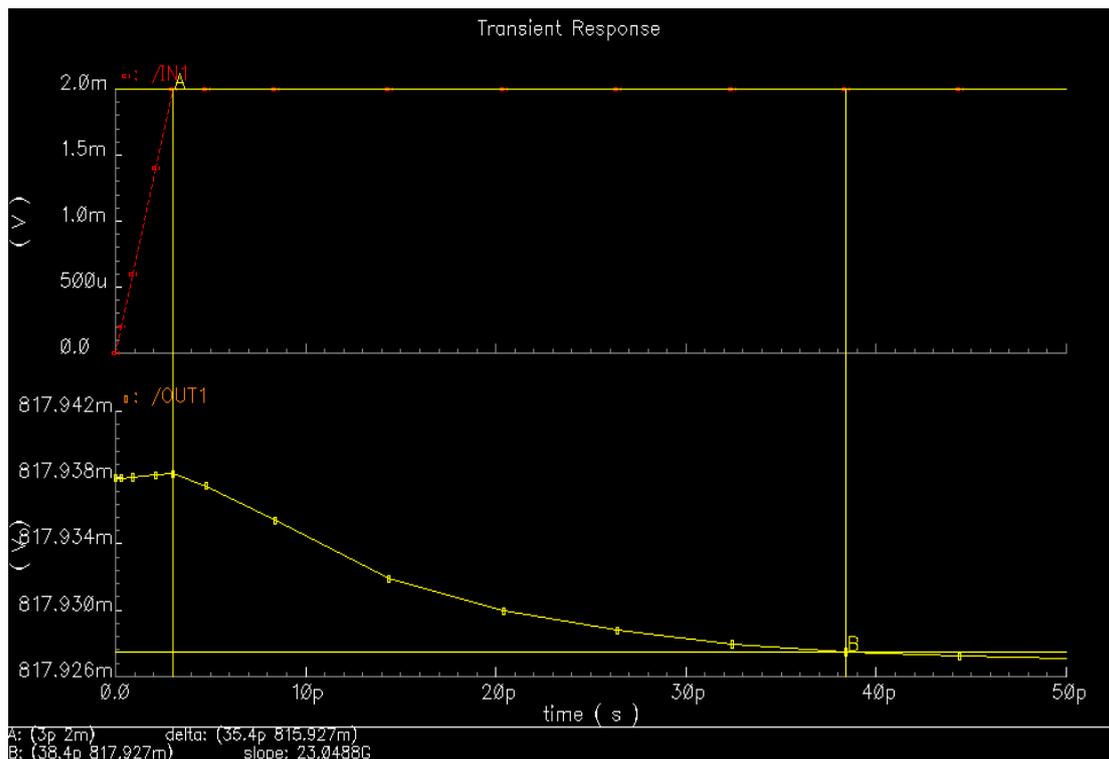


Fig. 10. Output Delay.

The delay in the output again depends on the voltage swing magnitude. For example, the output delay would increase if the output has to rise or fall to a larger magnitude as compared to a smaller magnitude. Hence the worst case delay is computed for a voltage swing of :

$$\Delta V_{in} = 1mV \quad (10)$$

It can be clearly seen from figure 4.5 that the delay from the transition of output 1 from high to a point where it attains steady state is:

$$Delay_{TOT} = 35.4ps \quad (11)$$

The voltage swing is:

$$\Delta V = 817.927 - 815.927 = 2mV \quad (12)$$

Thus the worst case delay for $\Delta V = 1mV$ is: $Delay_{\Delta V=1mV} = \frac{35.4}{2} = 17.7ps$

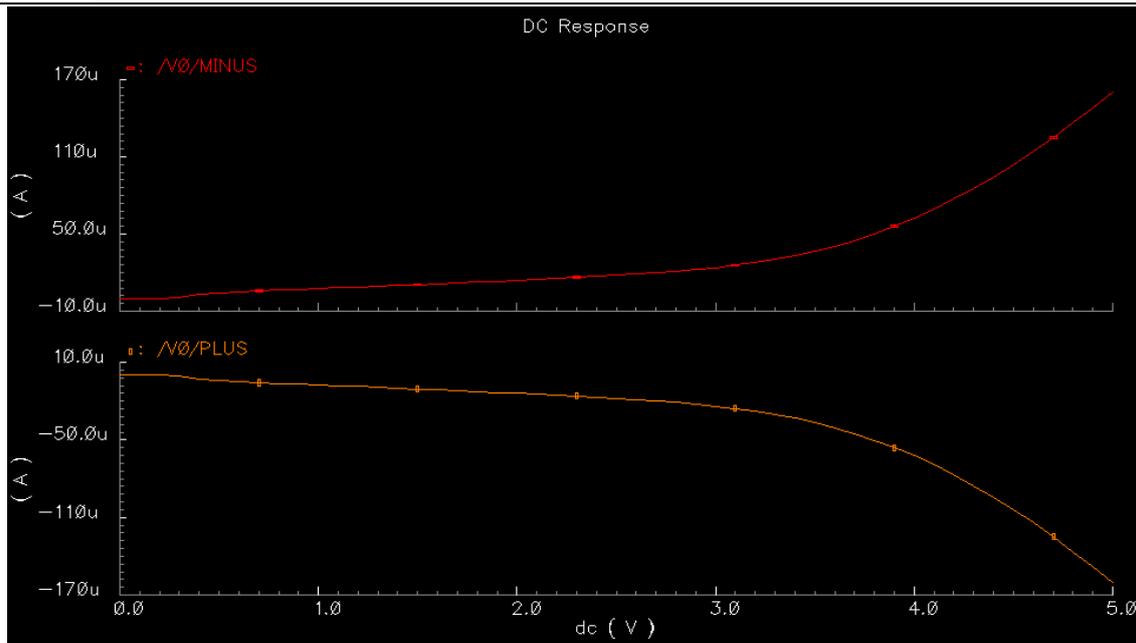


Fig. 11. DC Analysis of Proposed Comparator.

The figure above depicts the DC response of the proposed comparator. It can be seen that the dc voltage consumes time to reach the dc steady state voltage.

A comparative summary of the results for output parameters obtained by the proposed system and that of the previous work referred to is given below:

Table 2. Performance Comparison.

S. No	Comparator structure	Low voltage Low power Double Tail Comparator [10]	Proposed work
1	Technology CMOS	180nm	90nm
2	Supply Voltage	0.8V	1.2V
3	Maximum Sampling Frequency	2.4 GHz	3.33 GHz
4	Energy Per Conversion	24pJ	0.222198pJ
5	Worst Case Delay ($\Delta V=1\text{mV}$)	550ps	17.7ps

VI. CONCLUSION

The proposed work puts forth an double tail comparator that that minimizes the power consumption by using the comparison to take place only at the high level of the clock thereby saving considerable power. The comparator design has been implemented on 90nm CMOS technology on Cadence adhering to the state of the art standards laid down for VLSI design. The comparator designed here uses a shorting or switching transistor that reduces the dynamic range of the voltage swing from the entire value of supply voltage VDD to half of it thereby minimizing the delay of the comparator. The proposed comparator attains a sampling speed of 3.3 GHz at a supply voltage of 1.2V and is designed on 90nm. The power consumption in terms of energy per consumption is 0.222198 pico Joule and the worst case delay (for ΔV of 1 mV) is found to be 17.7 pico seconds. Apart from the supply voltage, the proposed comparator attains better output parameters compared to previously existing work [10].

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AUTHORS PROFILE

Priya Patne

Department of Electronics and Communication, TIT, Bhopal (India). email id: priya.patne2@gmail.com

Sandip Nemade

Department of Electronics and Communication, TIT, Bhopal (India). email id: nemadesandiptit@gmail.com