A Review of 65-Nm CMOS Constant Current Source with Reduced PVT Variation

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Abstract – Variations in process, supply voltage and temperature (PVT) have always been an issue in Integrated Circuit (IC) Design. In digital circuits, PVT fluctuations affect the switching speed of the transistors and thus the timing of the logic. This paper presents a method to compensate CMOS process-, voltage-, and temperature (PVT) variations. The circuit architecture is based on the embodiment of a process-tolerant bias current circuit and a scaled process-tracking bias voltage source for the dedicated temperature-compensated voltage to- current conversion in a pre-regulator loop.

Keywords – Current Reference, Line Sensitivity, Process Tracking, Temperature Compensation, Threshold Voltage VTH Circuit.

I. INTRODUCTION

The progressively high density of digital CMOS processes as well as new advances in Digital Signal processing is sparking a need to implement mixed signal systems on one chip. To realize one chip implementation an correct current reference is needed to perform conversions between the analog and digital domains.

The current reference circuit could be a key-stone is most electric equipment. Its sole purpose is to deliver an electrical current. Now, this can be simply finished a number of MOSFETs, but the most goal of this work is to develop one that has accuracy high enough to be used in additional precise systems.

Some systems like operational amplifiers, information converters and phase-locked loops believe current reference circuits to produce a correct and stable current supply.

Analog to Digital converters want a set reference for a measurement purpose for their sampling. Moreover, high performance analog circuits need a stable bias purpose across a wide varies of PVT conditions.

There has been a good deal of effort directed towards reducing the results of temperature on the output of those devices. References are currently being created that have very flat temperature responses and really little dependence on the facility offer voltage. These references will simply have temperature dependences less than 0.81% [1] over a 100°C vary. In several cases it's the accuracy of the particular output voltages of identical devices that limits the performance of the system. In regards to voltage compensation, it had been known for a short while and it still is one amongst the most used ways. We tend to call it a self-biasing circuit that has a offer independent voltage.

As we tend to go deeper into higher integration technologies, a wider vary of issues surface that require to be addressed. The most focus of this thesis are on the development of a current reference that features a five-hitter absolute preciseness over PVT conditions. One MOSFET or a BJT possess a large vary of parameters that change with PVT, so affecting its performance, stability and long run responsibility.

II. LITERATURE SURVEY

Dong Wang et al. [1] “A 65-nm CMOS Constant Current Source with Reduced PVT Variation”, A low-power constant current reference within the 65-nm CMOS is projected. By matching the temperature characteristic of the dedicated reference compensation voltage therewith of the output sense resistance within the op-amp-less VI convertor, a constant current reference with lower T.C. over the operational temperature vary and comparatively lower sensitivity to the overall PVT are achieved. With the embedded pre-regulator, this reference provides smart line sensitivity. This reference offers one amongst the lowest values of the sensitivity FOM with respect to reported counterparts.

Ken Ueno et al. [2] “A 1-μW 600-ppm/°C Current Reference Circuit Consisting of Sub-threshold CMOS Circuits”, developed an ultralow-power CMOS current reference circuit consisting of subthreshold MOSFET circuits and no resistors. The device generates a temperature and provides voltage compensated reference current. In this created a prototype chip that generates a 100-nA output current and demonstrated its operation by measurements. The TC and line regulation of the output current were 520 ppm/°C and 0.2%/V, respectively. The power dissipation was regarding one μW. Our circuits are helpful as a current reference circuit to be used in power-aware LSI applications, like RFID, implantable medical devices and smart sensor networks.

Tetsuya Hirose et al. [3] “A 46-ppm/°C temperature and process compensated current reference with on-chip threshold voltage monitoring circuit”, A CMOS current reference circuit has been developed in 0.35-μm CMOS method. The circuit consists of a voltage reference circuit, non-inverting electronic equipment and an output MOS transistor. The circuit generates a reference current independent of temperature and method variation. Temperature and method compensation were achieved by utilizing the zero temperature constant bias purpose of a MOSFET. Theoretical analysis and experimental results showed that the circuit generates a quite stable reference current of 18.4μA on the average. The temperature constant, load sensitivity and method sensitivity of the circuit were 46-ppm/°C, 1.5%/V and 4.4%, severally. The circuit will be used as a current reference circuit for high preciseness analog circuit systems.

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Byung-Do Yang et al. [4] “An Accurate Current Reference using Temperature and Process Compensation Current Mirror”, the area efficient correct current reference using the TPC-CM is projected. To calibrate the method variation, the proposed TPC-CM uses 2 binary weighted current mirrors which control the temperature constant and magnitude of the reference current. When the PTAT and CTAT current measurements, the temperature and method compensation switch codes of the TPC-CM are hold on within the non-volatile memory. Within the simulation, the TPC-CM reduces the method variation result to 0.52% from 19.7%. A current reference chip was invented with a 3.3V 0.35um CMOS method. The measured mark reference current has 0.42% variation for 20~1000C.

Wei Liu et al. [5] “A Resistor-Free Temperature-Compensated CMOS Current Reference”, A new temperature compensation scheme for current references circuits was described. The planned circuit exploits the edge difference between a nominal MOSFET device and a thick compound MOSFET transistor to generate the reference current while not using resistors. The circuit was designed during a normal 0.18 m CMOS method. Simulation results showed a temperature variation constant of 170 ppm/°C for the output current across a temperature vary of – 20 °C to 120°C and an output current variation of three across a supply vary of 2 V to 3 V. The results clearly illustrate that the planned circuit is compatible to each value effective and correct current supply across a large vary of PVT conditions and so may be integrated into future analog or digital circuits.

III. CURRENT REFERENCE ARCHITECTURE

A current architecture to generate a current source is shown below. This architecture refers only to the conversion between a voltage level and its current supply. This topology requires a band gap reference and works by controlling a certain dump of energy in node 1.

![Fig. 1. Current Reference Architecture](image)

During $\phi 1$, C1 charges to Vref. During $\phi 2$ this charge is dumped on node 1. Thus, the ripple voltage is -

$$\Delta V = -\left(\frac{2C1}{C1 + 2C2}\right) V_{ref}$$

The ripple voltage can be lowered by increasing the value of C2. A large C2 reduces at ripple at the expense of increased die area. The current delivered by the switched capacitor is approximately.

IV. VOLTAGE REFERENCE ARCHITECTURES

Voltage references are one in all the most used blocks in several PVT insensitive current references. There are a varieties of characteristics that are desirable in a very high quality voltage reference. It’s necessary that the reference will deliver a really constant voltage over many varying conditions. Changes within the supply voltage shouldn’t cause significant changes within the output voltage of the reference. The results of temperature on the output of the device ought to even be minimal. Finally, 2 identical references should have similar output characteristics, under a similar technology.

There are numerous totally different strategies of planning a voltage reference. Of these there are concerning 3 major classes that the various styles will constitute. These categories usually describe either the technology within which the reference is constructed or the method of deriving the constant output voltage.

In MOS technologies the most obvious method of derivation a reference is through the use of the edge voltage. Very correct references usually use buried Zener diodes. In strictly bipolar processes, the emitter base junction of a BJT is wont to derive the band gap voltage of silicon to be used as a reference voltage. Finally, it’s attainable to form bipolar transistors, in a very MOS method, that are equal to extract the band gap voltage of silicon. These are used with different MOS circuits to provide a reference voltage.

V. CONCLUSION

This brief study on the A 65-nm CMOS Constant Current Source with Reduced PVT Variation of very large scale integration system attempts to illustrate the recent research work that has been done in the field. Some research papers were discussed all focusing on different aspects and techniques of Reduced PVT Variation. In this paper brief study of voltage reference architecture and current reference architecture.

REFERENCES


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