

# Design of Hamming Neural Network for Real Time 0-9 Digit Recognition on HSPICE Synopsys Tool

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**Abstract** – This paper describes implementation of a real-time digit recognition. Artificial intelligence is integral part of a neural network which is based on mathematical equations and artificial neurons. The focus here is the implementation of the Artificial Neural Network Architecture (ANN) with on chip learning in analog VLSI for pattern recognition. It is a maximum likelihood classifier which can be implemented using VLSI. Modified Hamming neural network architecture is presented which accepts real time inputs as well as determine next close pattern with respect to input pattern. Modified digit recognition circuit was simulated using HSPICE level 49 model.

**Keywords** – ANN, HNN, VLSI, HSPICE.

## I. INTRODUCTION

Artificial neural network is widely used in variety of problems in the area of pattern recognition, signal processing, telecommunications, medical technical diagnosis, robotics and control systems [1]. ANN are implemented in digital, analog or mixed system architecture. Though ANN can be implemented on software for real time application, software based ANN are slower in execution in comparison to hardware based ANN [2].

Hardware implementation of ANN is more popular due to high speed of operation and low power. ANN has following features:

- Parallism: This makes neural network fast.
- Fault tolerant: The distributed data processing of ANN makes it easy to include necessary redundancy to implement a fault.
- Regular: ANN are composed of few different elements that are interconnected in a regular way. This makes the implementation easy [3].
- Adaptive: By programming, neural network can be made adaptable to new working condition.
- Asynchronous: This is an advantage while implementing electrical circuits because problem with spike on supply current worst case timing designs are eliminated [4].

Lippmann provides an introduction to the field of artificial neural networks by reviewing six important neural network models that can be used for pattern classification [5] as shown in figure 1.

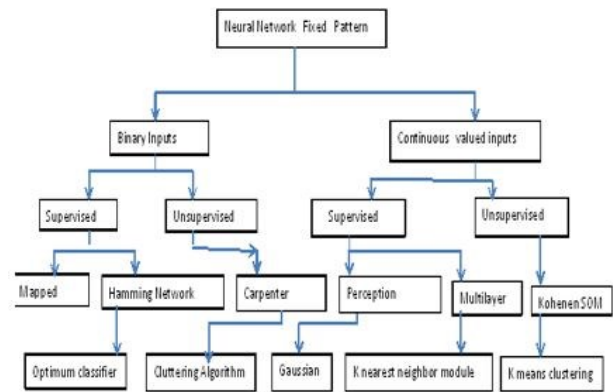


Fig. 1. Neural Network models

## II. HAMMING NEURAL NETWORK

It is a maximum likelihood classifier which selects from a group of exemplar pattern the closest one to an input pattern [6]. All patterns are presented in 1-D binary vector. When an input pattern  $P = (P_1, P_2, \dots, P_n)$  is presented to the network, hamming network calculates matching score between input pattern and each exemplar pattern.

$$W_i = (W_{i1}, W_{i2}, \dots, W_{in}) \text{ where } 1 \leq i \leq M$$

which is defined as

$$Msi = N - HD(P_i, W_i) = N - \sum_{j=1}^N |P_j - W_{ij}| \quad (1)$$

Where  $HD(P_i, W_i)$  is the hamming distance between input pattern  $P$  and exemplar pattern  $W_i$ .  $P_j$  is  $j$ th element of input pattern  $P (1 \leq j \leq N)$   $W_{ij}$  is  $j$ th element of exemplar pattern  $W_i$ . After this WTA operation is done to the matching score where only one winner is indicated by high level output.

$$V_i = \begin{cases} 1 & i = 1 \\ 0 & i \neq 1 \end{cases} \quad (2)$$

Advantages of hamming neural Network are number of connections required is less compared to other net as well as it.

Is acts as a minimum error classifier and Hamming net does not suffer from spurious outputs pattern which can produce 'no match' result [7]. It does not require digital to analog converter. Thus, it is most suitable to implement on CMOS technology [8].

## III. 0-9 REAL TIME DIGIT RECOGNITION CIRCUIT

The digit recognition is based on hamming neural network concept. The circuit determines winner pattern and the output will be high corresponding to that winning pattern whereas all other outputs will be inhibited to logic zero. When a trigger pulse is applied to circuit, the first winner output voltage will be inhibited to zero and the

output voltage corresponding to second winner (i.e. the most similar pattern having least hamming distance with respect to winner pattern) will be incited to rise to logic high level. So, we will be able to determine the most similar pattern using the same basic circuitry. Further, the pattern recognition circuit is altered so as to recognizing the data from real time patterns which takes input in the form of intensities [11]. The block diagram is as shown in figure 2.

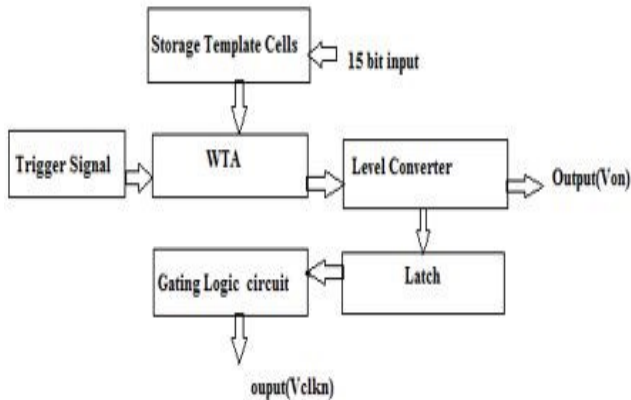


Fig. 2. Block diagram of modified digit recognition circuit

Additional features in circuitry are triggering signal generation circuit, gating logic circuit, latch circuit.

**Storage Template circuit:** These are 10 template storage sub circuit each one stores a single digit (0-9). Each digit is represented by 5x3 matrix form. This requires 15 inputs (in1 to in15). Corresponding voltages are generated from the intensities of inputs under recognition [12].

**Modified Winner Take all circuit (neuron cell):** It determines the closest template pattern with respect to input pattern. The circuit is modified with trigger signal generation circuit as shown in figure (1). A signal controlled NMOS is added in parallel to each neural cell which leads to inhibiting of that particular neural output when a triggering signal is applied across it. The triggering signal is applied when we want to determine the most similar pattern with respect to winning pattern.

**Trigger signal Generation:** The signal is generated when we want to determine the most similar pattern having least hamming distance.

#### Level Converter

This circuit converts neural output current in equivalent voltage. The operation is similar to old 0-9 level converter. It accepts input from WTA cells and converts in to equivalent voltage as Vo0 to Vo9 [13].

#### Latch Circuit

It is mainly used to latch output. It accepts input from level converter in the form of Vo0 to Vo9. Two complementary clock signals clkx and clkb are used to define the time at which input is to be latched. The outputs are V0, to V9.

#### Gating Logic Circuit

Logical ANDING is done between latch output and clock signal. The output signals are VCLK0 to VCLK9.

## IV. SIMULATION AND RESULTS

A snapshot of real time 0-9 digits is taken using low resolution camera. As shown in figure 3. Real time digit recognition circuit was simulated using HSPICE level 49 model parameters with version 3.1 at 180nm technology with VDD of 3V.

DC Analysis for pattern 0 is as shown in Table I where output voltage terminal Vo0 has voltage 2.63V showing HIGH status while all other output nodes are in Nano volts showing LOW status. When the input pattern perfectly match with stored template, maximum current flows showing maximum potential at that node and remaining node based on hamming distance, the potential value changes. Hence node X which corresponds to output terminal of 0 storing template cell has potential of 1.9V while all other are low. DC analysis of level converter shows output terminal corresponding to 0 Vo0 has voltage 2.63V while all other has Nano volts. This shows modified circuit is able to recognize '0' pattern. Table II shows the matching score and hamming distance for 0-9 digits.

Transient analysis was done for 100ns. Figure 3 shows the response. For input pattern '0', Vo0 sets to 2.63V while remaining all is set to LOW. Table 1 shows summary of modified digit recognition circuit.

Table I. DC ANALYSIS of REAL TIME DIGIT- 0

Rise Time and Fall Time delay	10Ps
Clk	100MHz
Vo0	2.63v
VDD	3v

Transient Analysis for digit 0 shows input pattern 0 is recognized first making Vo0 high. Later this output goes low as Vclk0 goes high. It determines next close pattern for digit 8.

Hence Vo8 goes high. Figure 4 shows the response. A delay of 0.35ns is observed to get second close pattern high as shown in figure 5.

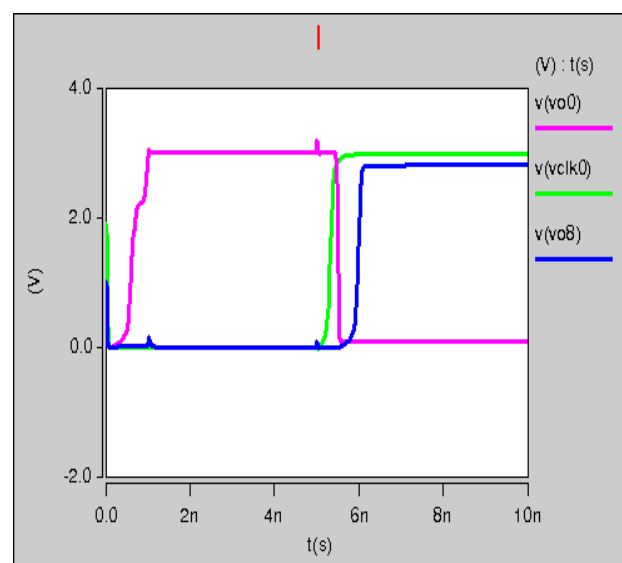


Fig. 5. Transient Analysis of real time digit 0 and its close pattern digit 8

Table II. Hamming Distance and matching score calculation for 0-9 digits

Pattern1	Pattern2	HD	ms
0	8	1	14
5	6	1	14
5	4	1	14
9	4	1	14
6	3	1	14
2	3	2	13
3	8	2	13
7	9	2	13

Table III. Summary of 0-9 Digit Recognition

S. No	Parameter	Values
1.	Technology	180nm
2.	Nature of operation	Asynchronous and non-sequential
3.	Power consumption	32mW
4.	Delay	0.4nS
5.	Area	Less
6.	Nature of input	Non-Binary
7.	Complexity	Less

### V. CONCLUSION

Hamming neural network is used for 0-9-digit recognition. The circuit was modified to accept real time inputs as well as to determine next close pattern with respect to input pattern. This type of circuit can be utilized by visual tracking system providing them ability to have backup recognition utility in case first recognized pattern proves to be incorrect. The circuit shows power consumption of 34mW and transient delay of 0.35nS. Given network can determine next close pattern only if hamming distance is less than 2. Given network can efficiently determine unique pattern only if the hamming distance is greater than 2 [15-17]. Table III shows summary of real time 0-9 digit recognition circuit.

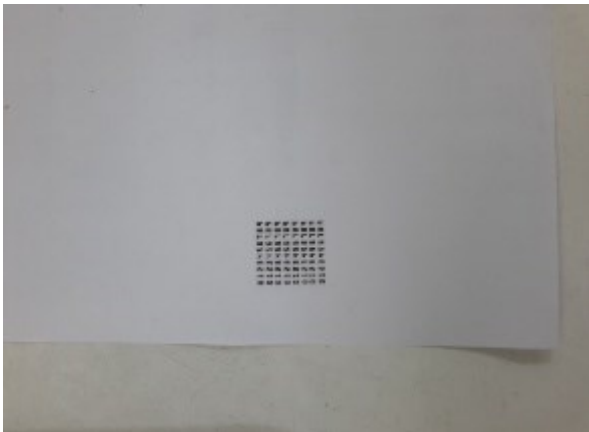


Fig. 3. Snapshot of Real Time 0-9 digit

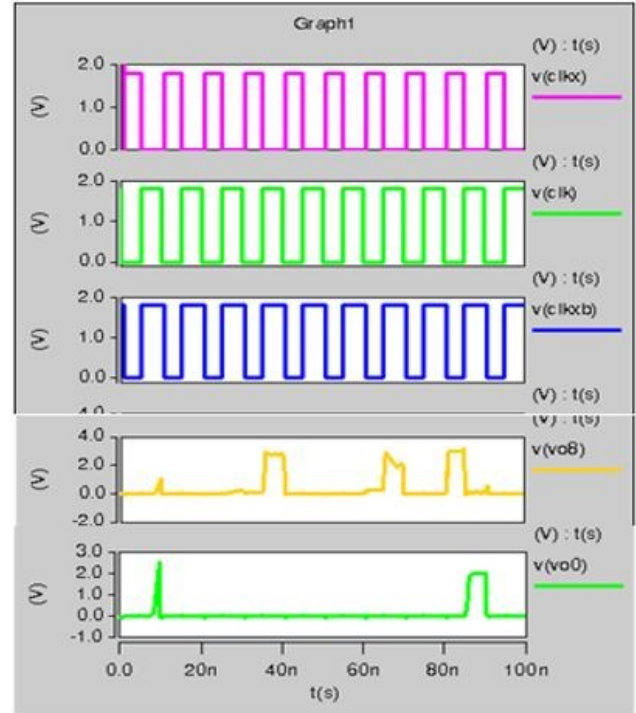


Fig. 4. Transient analysis of level converter

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