

Low Power SI Class E Power Amplifier for Healthcare Application

Wei Cai, Jian Xu, Shunqiang Wang

Abstract – The objective of this research was to design a 2.4 GHz class E Power Amplifier (PA), with 0.18um Semiconductor Manufacturing International Corporation (SMIC) CMOS technology by using Cadence software, for health care applications. The ultimate goal for such application is to minimize the trade-offs between performance and cost, and between performance and low power consumption design. This paper introduces the design of a 2.4GHz class E power amplifier which consists of cascade stage with negative capacitance. This power amplifier can transmit 16dBm output power to a 50Ω load. The power gain could reach 96 dBm and the total power consumption was 2.061 W. The performance of the power amplifier meets the specification requirements of the desired.

Keywords – About Cascade, Negative Capacitance, Class E, Power Amplifier, Healthcare.

I. INTRODUCTION

Wireless Sensor Networks (WSN) can be widely applied to solve a vast array of problems, under varied conditions[1]. By spatially distributing many devices to monitor the surrounding environment, WSNs can provide continuous, near-real time data over a large sampling area or population[2]-[9]. WSNs can provide considerable efficiencies to otherwise costly tasks [10]-[12]. For example, outpatient monitoring carries considerable cost, especially if applied to a large segment of the patient population. Cost-effective solutions can be established leveraging WSNs and the existing cellular communication infrastructure. Academic and industrial research is currently ongoing investigating such frameworks [13]-[23].

Due to current hardware limitations, healthcare application of WSNs are still in the early stages. Such devices require Food and Drug Administration (FDA) approval, which can be challenging and costly due to the requirement that the devices pass a number of safety tests. This has been historically challenging, with only a limited number of companies successfully building and fielding a device under full FDA approval [25].

WSNs consist of a number of networked elements, which are individually called sensor nodes. Sensor nodes contain a number of common hardware elements such as microprocessors, memory, batteries, MEMS sensors, antennas, etc [24]-[26]. A major design constraint for medical applications is that- since it is a consumer application - designs must meet functional requirements while being cost-effective [2]. In order to implement networks with a large number of nodes (for example with one node per patient), each node must be low cost. For many applications, WSN nodes have challenging power requirements, as well. Typically, each node must offer long working cycles without battery recharging. This drives most sensor node designs to be ultra-low power

devices. Achieving this low power performance at low cost are critical to making such sensor networks feasible[29].

In this pursuit, designs can reduce costs by leveraging the rapid development and widespread use of wireless systems. The wireless hardware industry, driven by global consumer demand, already strives for low cost, compact designs with flexible functionality. Transceivers systems are typically implemented in the Complementary Metal-Oxide Semiconductor (CMOS) technology. CMOS is a highly matured and well-understood technology. Advanced CMOS technologies can integrate the digital, analog and Radio Frequency (RF) components on a single, tiny chip.

The main challenge for such sensor node is the high power consumption of portable devices. A solution to this challenge is the integration of the portable devices' digital and RF circuitry into one chip.

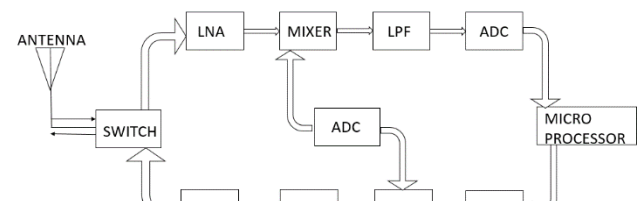


Fig. 1. Block diagram of a transmitter

The receiver will receive the signal and will also perform DSP processing after the data is sent out by the transmitter [26]. Fig. 1 is the transmitter diagram. It is desirable that the transmitter and receiver are low power devices. The direct-conversion transmitter is very popular for such applications, because it offers versatility, flexibility, spectral efficiency, and low complexity. These features make the transmitter simpler than the super-heterodyne transmitter. Small chip and circuit size, and low power consumption can be achieved with a direct-conversion transmitter architecture. For the front-end transmitter, the major objectives are 1) transmit RF signals and 2) recover the biosignal classification. This paper proposes a low power receiver design. This paper is mainly for the power amplifier design, since other portions of the circuit design are already discussed in the paper [28]. In order to meet the standards, the PA is designed as shown in Table I.

Table I: PA design requirement.

Parameter	Target(Unit)
Output Power	15 dBm
Power gain	50 dB
Stability	>1
S11	-10 dB

II. METHODS

Over the past 30 years, research on CMOS radio-frequency (RF) front-end circuits has progressed extremely quickly. The ultimate goal for the wireless industry is to minimize the trade-offs between performance and cost, and between performance and low power consumption design [29].

The cascode circuit with negative capacitance is shown in the Fig. 2. The advantage of this structure is that it provides less parasitic capacitance, since it allows the parasitic capacitance to be tuned at the driver stage. A shunt inductor instead of capacitor can also be inserted at the driver stage to filter out the unwanted parasitic capacitance, at the cost of wafer area [27].

As seen in Fig. 2, a negative capacitance can be implemented by a capacitor with a common gate amplifier. For class E power amplifiers, transistor M1 acts as a switch. Transistor M2 delivers high gain, when biased at saturation [28].

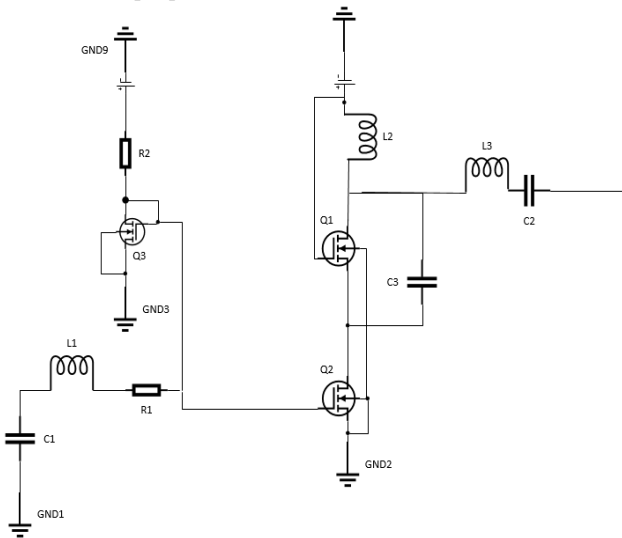


Fig. 2. Block diagram of a class E power amplifier

To get the optimum bias, small-signal simulation and 1dB compression point simulation are completed by their power output capability. Resulting design values can be shown in Table II.

Table II: 2.4GHz PA driver stage component.

Parameter	Target(Unit)
Q1,Q2	W/L=0.3um/0.6um(f=66,m=24)
Q3	W/L=0.8um/0.6um(f=4,m=2)
L1	36 nH (Q=20)
L2, L3	20 nH (Q=20)
C1	240 fH
C2	500 fH
R1	10.5 ohm
R2	3.8 Kohm

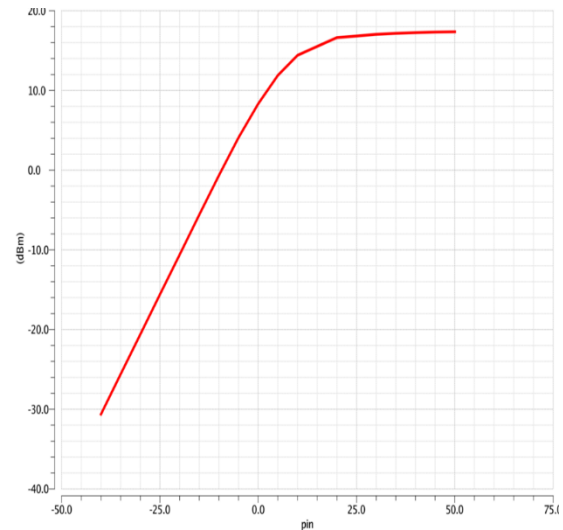
III. RESULTS

As seen in Fig. 3(a), the output power was 17 dBm. As seen in Fig. 3(b), the frequency is at 2.4 GHz the S11 is

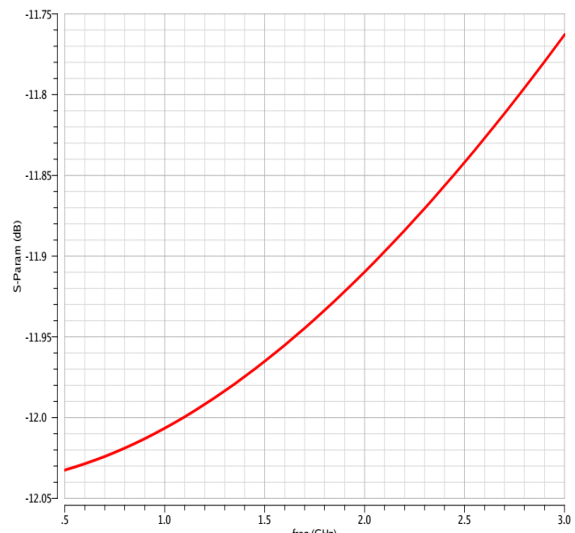
less than -10 dB, also, the total power of the PA is 2.061 W.

As seen in Fig. 4(a), Kf is larger than 1 for all frequencies from 1 to 3 GHz, so this circuit was totally stable. And Fig. 4(b) the power gain could reach 94 dB.

Since the technology nodes are becoming smaller and smaller, technology creates more challenges for analog/RF designers. For low supply voltage, it is not easy to design a very linear and high performance PA. Besides, accurate device modeling is needed, due to the leakage and process variations.



(a) Output power



(b) S11

Fig. 3. (a) Output power (b) S11

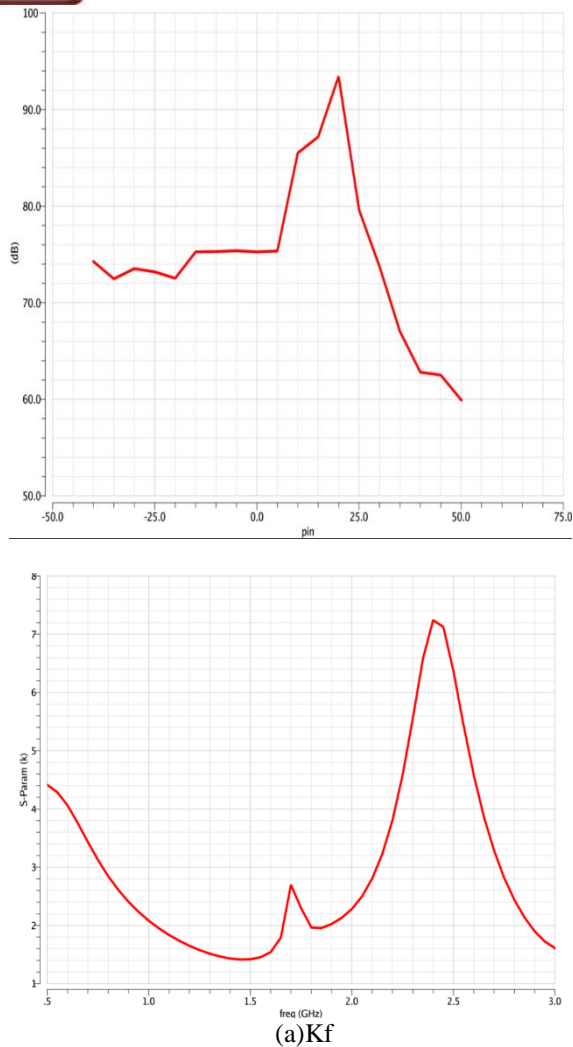


Fig. 4. (a) Kf (b) Power gain

IV. CONCLUSION

This paper describes the method of designing and simulating power amplifier using cadence software based on SIMC CMOS process 180nm technology. This PA is used for sensor networks. This research is still in the early stages of development of a low cost and low power device. In order to reach the performance that is needed, the PA process uses group III and IV elements. This circuit meets the scheduled requirements for the CMOS process, but it still has room to improve performance metrics. When the sensor is coupled with communications technologies such as mobile phones and the Internet, the sensor network constant information flow between individuals and their doctors. Such low cost and low power device can save a lot of hospitalization resources. To realize this, future improvement is needed.

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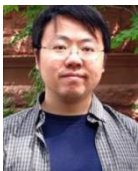
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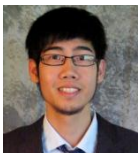
AUTHORS' PROFILES



Wei Cai is a graduate student at the University of California, Irvine, CA. She received her Masters degree from Dept. of Electrical Engineering, University of Hawaii at Manoa and Bachelor degree from Zhejiang University, China. Her research interests include device physics simulation, analog/ RF circuit design.



Jian Xu is an assistant professor at the Division of Electrical and Computer Engineering in the School of Electrical Engineering and Computer Science of Louisiana State University. He got his Ph. D. in Electrical Engineering at Yale University. He received a B. S. and a M. S. degree in Physics at Nanjing University, China. His research interest is in the Bioelectronics, Nanoelectronics and Nanomedicine, and Biomedical instrumentation for image-guided cancer surgery.



Shunqiang Wang received his Ph.D. in Mechanical Engineering from Lehigh University in 2016. His research interests are in the development of microfluidic devices and point-of-care devices for biomedical and chemical applications.