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CMOS Layout Design for Improved Latency Sequential Circuits

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***Abstract* – Microwind layout simulator is use to design the latches and flip flops and to calculates the parametric analysis such as power , switching delays, number of transistors, data and clock frequencies etc. The CMOS layouts are design and simulated for 8 bit asynchronous counter, 16 state mealy sequential circuit, 16 slot first in first out register for 8 bit data, and 4, 8 bit synchronize series connected XOR base CRC generator. The average power dissipation computed for these logic circuits are 22.29 µW, 32.66 µW, 78.12 µW, 60.27 µW and 120µW.**

***Keywords* – TG, FSM,FIFO, Synchronization, CRC.**

I. INTRODUCTION

The sequential circuits behavior depends on the basic cell called as latch and flip flop. These circuits operates in synchronous and asynchronous mode of operations. Depends on the behavior of clock signal, input change can affect the output at any instant in asynchronous sequential circuit and input change can affect the output at discrete intant of time in synchronous sequential circuits. The latches are transparent circuits are usually asynchronous sequential whereas flip flops are synchronous sequential circuit.

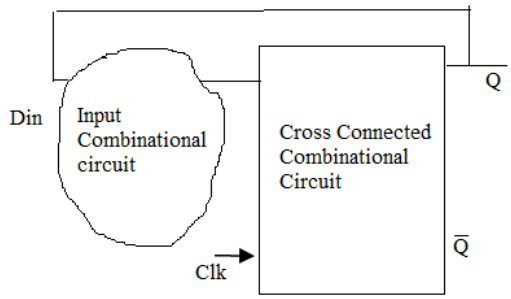

Fig. 1. Synchronize Sequential Circuit

The behavior of the master–slave flip-flop just described dictates that (1) the output may change only once, (2) a change in the output is triggered by the negative edge of the clock, and (3) the change may occur only during the clock's negative level. The value that is produced at the output of the flip-flop is the value that was stored in the master stage immediately before the negative edge occurred . It is also possible to design the circuit so that the flip-flop output changes on the positive edge of the clock. This happens in a flip-flop that has an additional inverter between the Clk terminal and the junction between the other inverter and input En of the master latch. Such a flip-flop is triggered with a negative pulse, so that the negative edge of the clock affects the master and the positive edge affects the slave and the output terminal [1,2].

II. COUNTER DESIGN

A register that goes through a prescribed sequence of states upon the application of input pulses is called a counter . The input pulses may be clock pulses, or they may originate from some external source and may occur at a fixed interval of time or at random. The sequence of states may follow the binary number sequence or any other sequence of states. A counter that follows the binary number sequence is called a binary counter . An n -bit binary counter consists of n flip-flops and can count in binary from 0 through 2^n - 1. Counters are available in two categories: ripple counters and synchronous counters. In a ripple counter, a flip-flop output transition serves as a source for triggering other flip-flops. In other words, the C input of some or all flip-flops are triggered, not by the common clock pulses, but rather by the transition that occurs in other flip-flop outputs. In a synchronous counter, the C inputs of all flip-flops receive the common clock. A binary asynchronous counter consists of a series connection of complementing flip-flops, with the output of each flip-flop connected to the C input of the next higher order flip-flop. The flip-flop holding the least significant bit receives the incoming count pulses.

Our design counter circuits can be built using T flip-flops because the toggle feature is naturally suited for the implementation of the counting operation. We can design this flipfop by connecting the Qn output to the D input of Master slave D flipflop shown in above figure. Fig 2 shows four bit counter capable of counting from 0 to 15. The clock inputs of the four flip-flops are connected in cascade. The input of each flip-flop will be toggled at each negative edge of its clock. We are assuming that the purpose of this circuit is to count the number of pulses that occur on the primary input called Clock. Thus the clock input of the first flip-flop is connected to the Clock line. The other three flip-flops have their clock inputs driven by the Q output of the preceding flip-flop. Therefore, they toggle their state whenever the preceding flip-flop changes its state from Q = 1 to Q = 0, which results in a positive edge of the Q signal [2,4].

The asynchronous counter design using these transmission gate (TG) base flip flop is shown in fig 2. It consist of four flip flops design with 8 transmission gates and 28 NOT logic gates comprises of 36 NMOS and 36 PMOS which is less than the number of transistors of conventional four bit asynchronous counter design. The

conventional counter is design with 72 NMOS and 72 PMOS transistors.

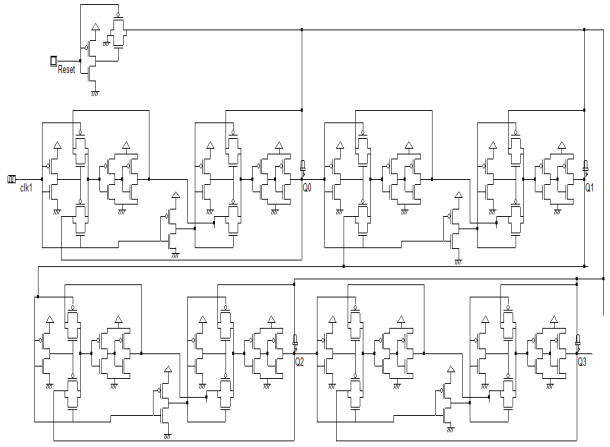

Fig. 2. Four bit Asynchronous Counter using transmission gate

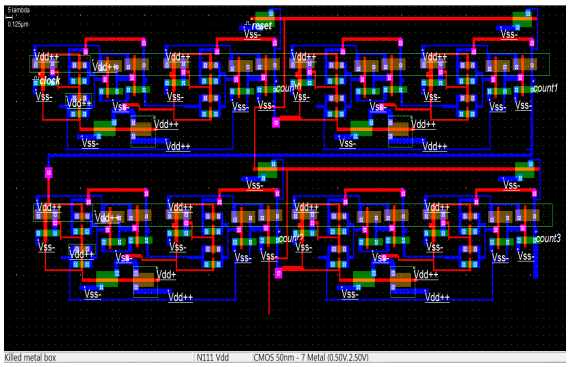

Fig. 3. CMOS layout Design for 4 bit counter

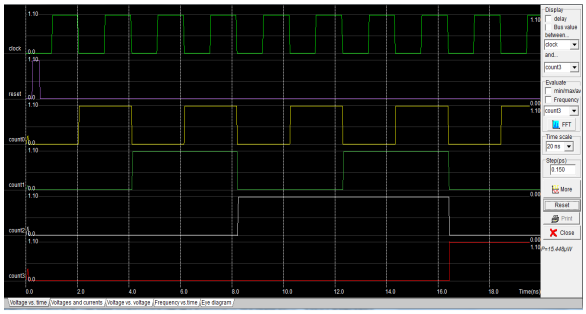

Fig. 4. Timing Simulation of 4 bit counter

The 8 bit transmission gate base counter consist of 32 transmission gates and 56 NOT logic gates. The total 88 NMOS and 88 PMOS transistors. A one transmission gate along with inverter is use to reset the content of counter. The out put of this reset logic circuit is connected to the output port Q of each flip flops and the input of its transmission gate is connected to ground supply. On the arrival of reset signal the reset TG is turn ON and the output of each flip flop is connected to the ground supply through this reset circuit. When the reset signal is inactive, then the counter starts to increment its state at each negative edge trigger of clock signal.

III. Finite State Machine

A finite state machine (FSM) is an abstract model describing the synchronous sequential machine and its spatial counterpart, the iterative network. It is the basis of understanding and development of various computation structures. The behaviour of finite state machine is describe as a sequence of events that occur at discrete instant, designated as t=1,2,3,4,…. Let consider that the machine has been receiving input signal and has been responding by producing output signal. At time t when input signal is applied then its output depends on the input signal and status of its past output value.

The most general model of a sequential circuit has inputs, outputs, and internal states. It is customary to distinguish between two models of sequential circuits: the Mealy model and the Moore model. In the Mealy model, the output is a function of both the present state and the input. In the Moore model, the output is a function of only the present state. A circuit may have both types of outputs.

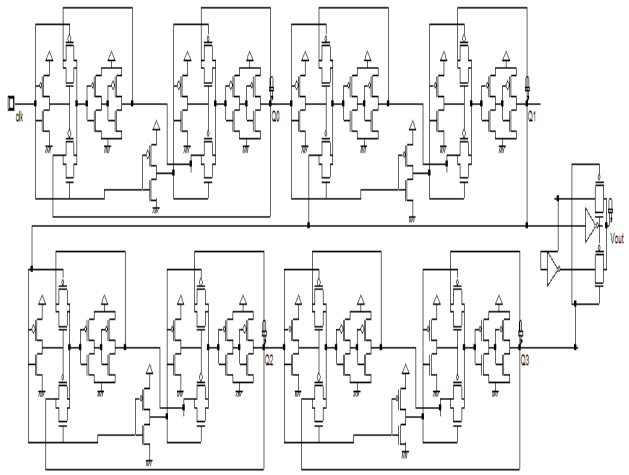

Fig. 5. Four bit Finite state Machine

The two models of a sequential circuit are commonly referred to as a finite state machine, abbreviated FSM. The Mealy model of a sequential circuit is referred to as a Mealy FSM or Mealy machine. The Moore model is referred to as a Moore FSM or Moore machine. In a Moore model, the outputs of the sequential circuit are synchronized with the clock, because they depend only on flip-flop outputs that are synchronized with the clock. In a Mealy model, the outputs may change if the inputs change during the clock cycle. Moreover, the outputs may have momentary false values because of the delay encountered from the time that the inputs change and the time that the flip-flop outputs change. In order to synchronize a Mealy-type circuit, the inputs of the sequential circuit must be synchronized with the clock and the outputs must be sampled immediately before the clock edge. The inputs are changed at the inactive edge of the clock to ensure that the inputs to the flip-flops stabilize before the active edge of the clock occurs. Thus, the output of the Mealy machine is the value that is present immediately before the active edge of the clock [2,3,4].

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IV. First in First out Shift Register (FIFO)

A register capable of shifting the binary information held in each cell to its neighbouring cell, in a selected direction, is called a shift register. The logical configuration of a shift register consists of a chain of flip-flops in cascade, with the output of one flip-flop connected to the input of the next flip-flop. All flip-flops receive common clock pulses, which activate the shift of data from one stage to the next. Higher data-transfer rates have dictated the need for FIFOs to evolve into clocked architecture wherein data is moved in and out of the device with synchronous controls. Each synchronous control of the clocked FIFO uses enable signals that synchronize the data exchange to a free-running (continuous) clock. Since the continuous clocks on each port of a clocked FIFO can operate asynchronously to each other, internal status signals indicating when the FIFO is empty or full can change with respect to either clock. To use a status signal for port control, it is synchronized to the port's clock on a clocked FIFO. Clocked FIFOs have become popular for relieving bottlenecks in high-speed data traffic. Data transfers for many systems are synchronized to a central clock with read and write enables. These free-running clocks can be input directly to a clocked FIFO with the same enables controlling its data transfer on the low-to-high transition of the clock. Reducing the number of clocks keeps the interface simple and easy to manage. Extra logic is needed to produce a gated pulse when using a FIFO that accepts a clock only for a data transfer request. The generated clock signal is a derivative of the master clock with a margin of timing uncertainty.

A basic four-bit shift register can be constructed using four D flip-flops, as shown below. The operation of the circuit is as follows. The register is first cleared, forcing all four outputs to zero. The input data is then applied sequentially to the D input of the first flip-flop on the left (FF0). During each clock pulse, one bit is transmitted from left to right. The least significant bit of the data has to be shifted through the register from FF0 to FF3. A basic four-bit shift register can be constructed using four D flip-flops, as shown below. The operation of the circuit is as follows. The register is first cleared, forcing all four outputs to zero. The input data is then applied sequentially to the D input of the first flip-flop on the left (FF0). During each clock pulse, one bit is transmitted from left to right. The least significant bit of the data has to be shifted through the register from FF0 to FF3. In order to get the data out of the register, they must be shifted out serially. This can be done destructively or non-destructively. For destructive readout, the original data is lost and at the end of the read cycle, all flip-flops are reset to zero. To avoid the loss of data, an arrangement for a non-destructive reading can be done by adding two AND gates, an OR gate and an inverter to the system.

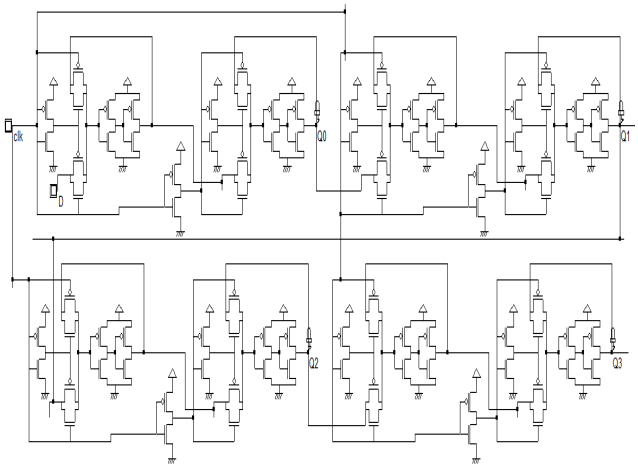

Fig. 6. First in First out Shift Register

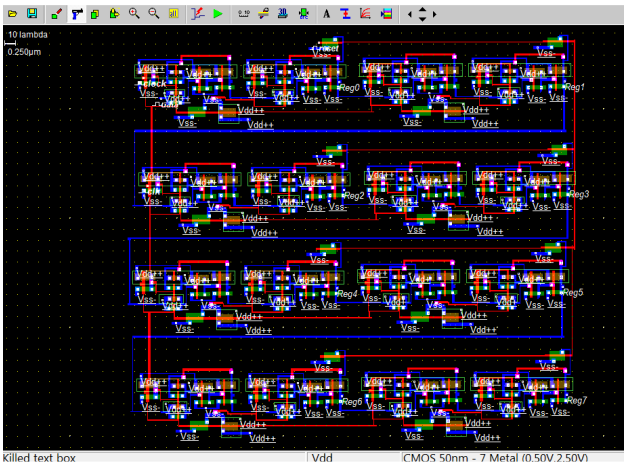

Fig. 7. Layout Design for synchronize 16-slot FIFO, 8-b data item

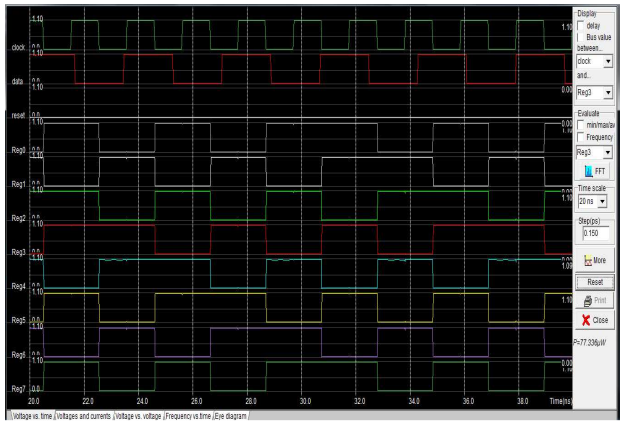

Fig. 8. Timing simulation of synchronize 16-slot FIFO, 8-b data item

The serial input determines what goes into the leftmost flip-flop during the shift. The serial output is taken from the output of the rightmost flip-flop. Sometimes it is necessary to control the shift so that it occurs only with certain pulses, but not with others. As with the data register discussed in the previous section, the clock's signal can be suppressed by gating the clock signal to prevent the register from shifting. A preferred alternative in high speed circuits is to suppress the clock action, rather than gate the clock signal, by leaving the clock path

unchanged, but recirculating the output of each register cell back through a two-channel mux whose output is connected to the input of the cell [4,5,6].

Table 1. Comparative Analysis with related work in [1]

Module Design		[1]		This Work	
Data Path	Discription		Power dissipation (μW)		Power dissipation (μW)
Counter	8-b binary counter		32.2		22.29
CRC8	4-b crc 8-b data item		187.2		60.27
CRC16	8-b crc 16-b data item		349.7		120
fsm16	finite state machine with 16 states		32.9		32.66
fifo16	16-slot FIFO, 8-b data item		325.7		78.12

V. CONCLUSION

Synchronization latency can be avoided in individual cases when the communicating clocks share a timing relationship. This is because it becomes possible to detect when clock data variance might occur and avoid sampling the input in the neighbourhood of hazardous intervals. Using faster flip-flops decreases the switching times of the flip-flop, which in turn reduces the time window that the flip-flop is susceptible to non synchronization. When the input frequency is decreased, the probability of the input changing during the switching time also decreases. Micro wind layout simulator is use to design the latches and flip flops and to calculates the parametric analysis such as power , switching delays, number of transistors, data and clock frequencies etc. The CMOS layouts are design and simulated for 8 bit asynchronous counter, 16 state mealy sequential circuit, 16 slot first in first out register for 8 bit data, and 4, 8 bit synchronize series connected XOR base CRC generator. The average power dissipation computed for these logic circuits are 22.29 μW, 32.66 μW, 78.12 μW, 60.27 μW and 120μW.

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