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An Improved Architecture for Multiple-Order Single-Bit Quantizer Based Over-Sampled Delta-Sigma Modulators

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***Abstract* – A modified alternative switched capacitor discrete-time architecture than that of its regular architecture (a chain of integrators with distributed feedback)for Multiple-Order, Single-bit Quantizer based Over-Sampled Delta-Sigma Modulator (DSM) is proposed. The proposed circuit consists of single-order architecture but includes an added feedback path circuit to establish multiple-order noise-shaping function. This proposed architecture requires only one OP-AMP irrespective of the number of order and provides approximately the same NTF function and slightly better SNR value than that of regular multiple-order architecture. The advantage of having only one OP-AMP is that it allows us to go for high speed and reduced static power dissipation. The cost we are paying for this proposed architecture is that we would need more number of sampling and evaluation pulses than regular architecture and also faces mismatching error but if all the input sampling capacitances in the circuit have equal % variation in the process mismatching then this problem is somewhat alleviated. Theover-sampled delta-sigma modulators for digital audio using the above said switched capacitor, discrete time-domain architecture are designed and developed. The technology used is 130nm, 1.2v, CMOS process. The SPICE simulation shows promising result in SNR for the proposed architecture than that of regular architecture. The attained SNR value using SPICE for the proposed architecture based third order DSM is 91dB whereas for the regular architecture based third order DSM is 83dB for a sine-wave input.**

***Keywords* – Delta-Sigma Modulators, Data Converters, Switched-Capacitor Circuits, Op-Amp, Comparator, SPICE Simulation, SNR.**

I. Introduction

The over-sampled delta-sigma modulators [1]-[4] find widespread applications in precision data converters. The key point in such modulators is that output of the modulator signal should get settled well within half of the inverse of the sampling rate at each evaluation phase. This poses a strict limitation on the high-speed data converters. The regular (a chain of integrators with distributed feedback) switched-capacitor architecture for DSMs uses multiple op-amps and switched capacitor circuits to realize higher-order NTF noise-shaping function. But it requires a considerable amount of time for the output signal of the modulator (to the quantizer) to get settled at each evaluation phase time due to the number of op-amps and switched capacitor circuit RC timings.

There are many circuit topologies for the chain of integrators based architecture which have been successfully used in delta-sigma modulators. For example, a chain of integrators with distributed feedback [5], chain of integrators with distributed feedback and distributed feedforward input paths (CIFB) [5], [7], chain of integrators with distributed feedback, distributed feedforward input paths and local resonators feedbacks (CRFB) [5], chain of integrators with weighted feedforward summation (CIFF) [5]-[7], chain of integrators with feedforward summation and local resonator feedbacks (CRFF) [6].

One different approach which relies on the cancellation rather than the filtering of the quantization noise to realize a modulator is to use a cascade-type structure where the overall higher-order modulator is constructed using lower-order ones. This arrangement is called MASH architecture [8] but uses multiple op-amps to realize the circuit. One more approach to realize the modulator is to use error-feedback structure similar to the one in the proposed architecture [9]-[10] but still uses more than one op-amp for circuit implementation and also faces mismatching error.

This paper presents a simple technique to the multiple-order single-bit delta-sigma modulators wherein it uses only one op-amp but requires more number of sampling and evaluation pulses apart from the main sampling pulse. It establishes approximately the same NTF (noise transfer function) and STF (signal transfer function) and noise-shaping and provides slightly better SNR values than regular architecture. The advantages gained from the proposed architecture is that of higher speed and reduced static power dissipation but faces mismatching process error but if all the input sampling capacitances of the switched-capacitor circuit have strictly equal % variation in the process mismatching, then this problem is somewhat reduced. An over-sampled DSM with the present architecture has been designed with second-order and third- order noise-shaping for digital audio and the SPICE simulated results are compared to the regular architecture based DSMs.

The paper is organized as follows. The next section II describes the proposed architecture for the second-order and third-order single-bit quantizer based DSMs and the limitations of the technique. The section III describes about the switched capacitor circuits, op-amp and the comparator used in the architecture and their drawbacks. The section IV presents an example design circuit for 130nm, 1.2v CMOS process and the results including SPICE are presented. The section V summarizes the work involved in this paper.

II. The Proposed Architecture of DSM

The generalized multiple-order single-bit over-sampled DSM architecture for ADCs proposed in this paper is shown in Fig.1. A linearized model for the quantizer is assumed.

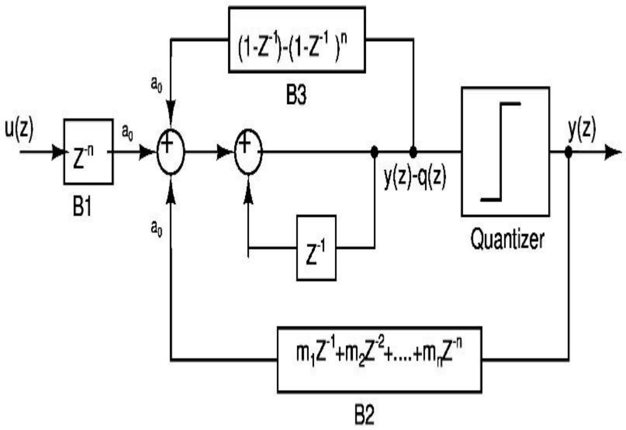

Fig.1. Proposed architecture of DSM

The proposed DSM has mainly three blocks. The first block, B1[z] provides the sampled and z^{-n} delayed input to the integrator. The second block, B2[z] gives the weighted delayed outputs (y[z]) in the feedback path. The third block, B3[z] provides the necessary multiple-order noise-shaped NTF numerator function. In Fig.1, we have,

$$B1[z] = z^{-n}u[z] \quad (1)$$

$$B2[z] = \left(m_1 z^{-1} + m_2 z^{-2} + ...m_n z^{-n}\right)y[z] \quad (2)$$

$$B3[z] = \left[\left(1-z^{-1}\right) - \left(1-z^{-1}\right)^n\right]\left(y[z]-q[z]\right) \quad (3)$$

Where u[z] is the input signal, y[z] is the modulator output and q[z] is the quantization noise signal. For example in a second-order and third-order noise-shaped modulators, B3[z] are given by,

$$B3\_second[z] = \left(z^{-1} - z^{-2}\right)\left(y[z]-q[z]\right) \quad (4)$$

$$B3\_third[z] = \left(z^{-3} - 3z^{-2} + 2z^{-1}\right)\left(y[z]-q[z]\right) \quad (5)$$

For a second-order modulator from Fig,1, the NTF and STF are given by the following expressions.

$$NTF[z] = \frac{a_0\left(1-z^{-1}\right)^2}{D[z]} \quad (6)$$

$$STF[z] = \frac{a_0 z^{-2}}{D[z]} \quad (7)$$

Where D[z] is given by,

$$D[z] = a_0\left(1-z^{-1}\right) - a_0\left(m_1 z^{-1} + m_2 z^{-2}\right) - a_0\left(z^{-1} - z^{-2}\right) \quad (8)$$

$$\text{Where } a_0 = a_{0s}\left(\frac{1 \pm p_1}{1 \pm p_2}\right) \quad (9)$$

Where a_{0s} is the scaling factor without any process variation in the capacitances and p_1 accounts for the variation in each input sampling capacitance due to process mismatching factor and p_2 accounts for the variation in the output feedback capacitance of the op-amp due to process mismatching factor. It is to be noted that all the input sampling capacitances should have equal variation in the process mismatching. In practice this may not be the case but at least the input sampling capacitances present in the block B3 should strictly meet this condition to avoid any mismatching error problem in the dynamic performance.

The frequency response of NTF and STF for the typical second-order modulator (for m_1=-1, m_2=0)as an example are given approximately by (the poles of NTF[z] all lies inside the unit circle for m_1=-1 and m_2=0 for this case),

$$NTF(s) = \frac{s^2T^2}{\left(s^2T^2 + sT + 1\right)} \quad (10)$$

$$STF(s) = \frac{1}{\left(s^2T^2 + sT + 1\right)} \quad (11)$$

The time T is the basic sampling clock period. T=1/f_s, where f_s is the sampling rate.

Similarly the NTF(z) and STF(z) for a third-order over-sampled modulator are given by,

$$NTF(z) = \frac{a_0\left(1-z^{-1}\right)^3}{D[z]} \quad (12)$$

$$STF(z) = \frac{a_0 z^{-3}}{D[z]} \quad (13)$$

Where D[z] is given by,

$$D[z] = a_0\left(1-z^{-1}\right) - a_0\left(m_1 z^{-1} + m_2 z^{-2} + m_3 z^{-3}\right) - a_0\left(z^{-3} - 3z^{-2} + 2z^{-1}\right) \quad (14)$$

Where a_0 is given by equation (9).

The frequency responses for this third-order modulator (m_1=-2, m_2=2, m_3=-1) as an example are approximately given by (the poles of NTF[z] all lies inside the unit circle for this third-order),

$$NTF(s) = \frac{s^3T^3}{s^3T^3 + 2s^2T^2 + 2sT + 1} \quad (15)$$

$$STF(s) = \frac{1}{s^3T^3 + 2s^2T^2 + 2sT + 1} \quad (16)$$

As noted in the above equations, the NTF and STF approximately form the same functions as that of regular architecture but the proposed architecture uses only one op-amp. The various sampling and evaluation pulses used in the proposed circuit in implementing B1[z], B2[z] and B3[z] blocks are shown in the next section.

III. Circuit Design

The blocks B1[z], B2[z] and B3[z] described in the previous section require more number of sampling and evaluation pulses other than main sampling clock as illustrated in Fig.2. In Fig.2, pulses P1 and P2 are

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sampling and evaluation main clocks. In Fig.2, the pulses PS1_1 and PS2_1 form one set of pulses namely odd sampling phase and even evaluation clocks. Similarly PS1_2 and PS2_2 form second set of pulses namely even sampling phase and odd evaluation phase. These four set of pulses (PS1_1, PS2_1, PS1_2, PS2_2) are used to obtain the second order delay namely, z^{-2} as shown in Fig.3. The Fig.3 also has an integrator $(1\text{-}z^{-1})^{-1}$ along with the second-order delay. The realized output of the fully differential integrator is shown in Fig.3.

Similarly to obtain z^{-3}, six set of pulses are required namely PT1_1, PT2_1, PT1_2, PT2_2, PT1_3, PT2_3. The Fig.3 can be modified to include these pulses to obtain z^{-3} along with integration. In the general case, the number of pulses required to obtain z^{-n} increases more and more for the n^{th} order delay. This is a main drawback in the proposed circuit design. These pulses can be obtained from the main clocks P1 and P2 through simple counters.

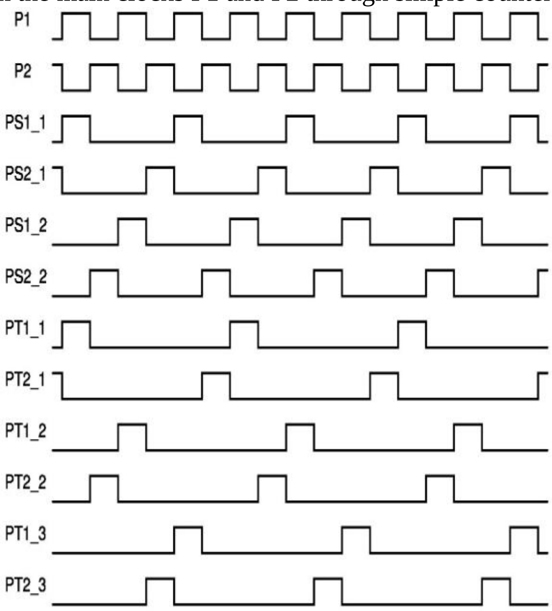

Fig.2. Sampling and evaluation pulses as required in the proposed DSM.

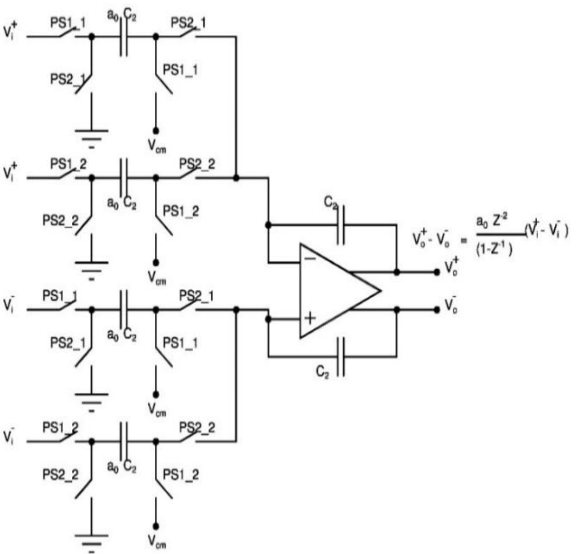

Fig.3. Delayed integrator using sampling and evaluation pulses as in Fig.2.

The proposed architecture uses only one op-amp as shown in Fig.1. The advantages of this architecture is that of higher speed and reduced static power dissipation. The circuit used for the op-amp is shown in Fig.4. It is a fully differential folded-cascode op-amp [2] with common-mode feedback. If the op-amp is fast enough to allow the circuit to settle completely, then the speed can be achieved more. As the number of op-amps increases with the multiple-order noise-shaping NTF function, the op-amps really have to be faster in the regular architecture. This problem is somewhat can be reduced with the proposed architecture with just only one op-amp. The cascode arrangement in Fig.4 yields a high-speed op-amp that has the low-frequency open-loop gain of a two-stage amplifier. The folded-cascode circuit in Fig.4 has a greater output swing than a direct stack of transistors. The output voltage swing of the op-amp is determined by the cascode P devices, P3 and P4, in the positive direction, and by the cascode N devices, N3 and N4, in the negative direction. For the greater speed N-channel devices are chosen for the input pair. To maintain stability, all non-dominant poles must occur at frequencies higher than the unity-gain bandwidth of the op-amp. The common-mode feedback circuitry in Fig.4 changes the CM output voltage by controlling the gates of N1 and N2. The CM op-amp compares the average of the op-amp outputs to the desired centering point. If the op-amp outputs are too high, more of I_{P7} will flow through P5 rather than P6. This will increase the gate voltage of N1 and N2, pulling the outputs down. The average of op-amp outputs can be derived from a high resistive divider without loading.

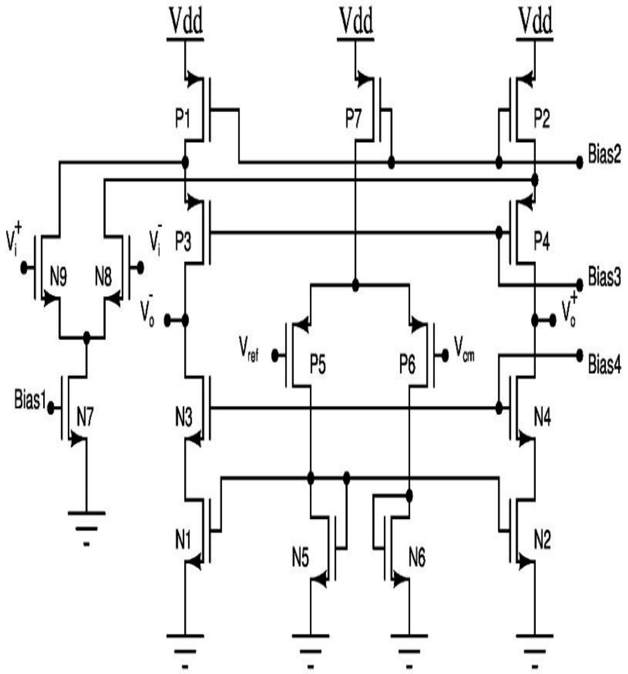

Fig.4. Fully differential folded-cascode Op-amp with CM feedback.

The second major component of the modulator is the comparator. The performance of the modulator is relatively insensitive to comparator offset and hysteresis since the effects of these impairments are attenuated by the

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multiple-order noise-shaping that attenuates the large quantization noise. The regenerative latch as shown in Fig.5 has been used to implement the comparator [12]. In this latch, the cross-coupled devices M2A-M2B and M3A-M3B are strobed at their drains. The latch is strobed at the beginning of the sampling phase when P1 transitions from low to high. The latch is reset at the end of the sampling phase and the result of the comparison is stored in an RS latch (not shown). The switching threshold of the output inverters in Fig.5 is set low intentionally. In the event that the comparator is unable to come to a decision before P1 falls, the result of the previous comparison will remain in the RS latch.

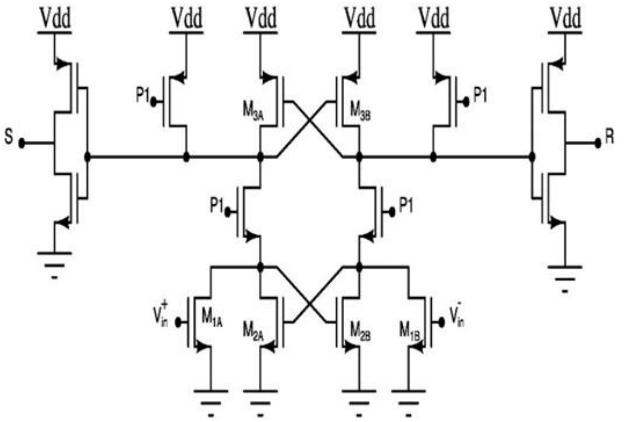

Fig.5. Regenerative feedback Comparator.

IV. The Results

The process used in the following example design is 130nm, 1.2v IBM CMOS process. A second-order and third-order single-bit quantizer based modulators for a digital audio are studied in this paper. The over-sampling ratio used is 128. The sampling rate is 5.6448MHz. A pure sine-wave signal with an input frequency of 11.025KHz and an amplitude of 150mv is used to get power spectral density (PSD) plot. The output of the 1-bit DAC in the feedback path is ±200mv. The CM voltage for the op-amp is 0.625v. A DAC is placed at the output of the comparator which averages the 128 previous states of the comparator for studying the PSD plot. This DAC is equivalent to an averaging FIR Since filter.

The STF and NTF functions with respect to normalized frequency were studied using a C-program and are shown in Fig.6 and Fig.7 for the typical second-order (Equations (10) and (11)) and for the typical third-order (Equations (15) and (16)) architectures respectively.

The obtained integrated output spectrum of power spectral density plot (PSD) with respect to normalized frequency for a second-order noise shaping using the proposed architecture by SPICE simulation and after FFT and for the example design studied in this paper is shown in Fig.8. Only 2680 cycles of basic sampling clock were used to get the spectrum plot due to time constraint using a laptop computer. The values of PSD are accumulated and scaled by 1/ (N.NBW) where NBW is the noise bandwidth [1] and N is the number of cycles used. The signal bandwidth points are not included in performing integration. From this we obtain SPICE simulated SNR of 89dB whereas for the second-order regular architecture is 81dB. Similar plot for the third-order using proposed architecture is shown in Fig.9 and from this we get a SNR of 91dB whereas for the third-order regular architecture is 83dB.

The SPICE simulated SNR plot with input amplitude was studied and is shown in Fig.10 for a second-order noise shaping (using example studied in this paper). Similar one for the third-order is shown in Fig.11. Please note that only few SPICE simulations were carried out in getting the plots Fig.10 and Fig.11 due to time constraints.

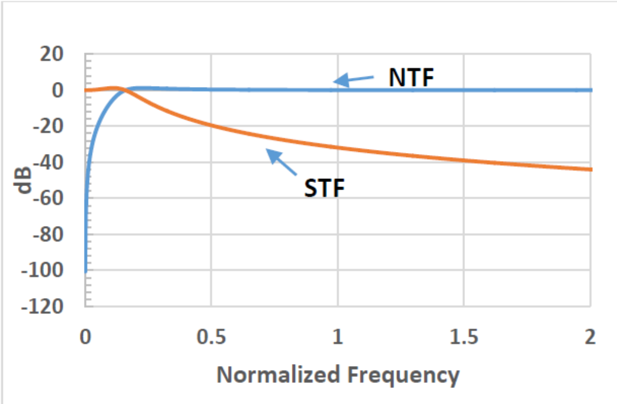

Fig.6. NTF and STF functions for the second-order proposed architecture.

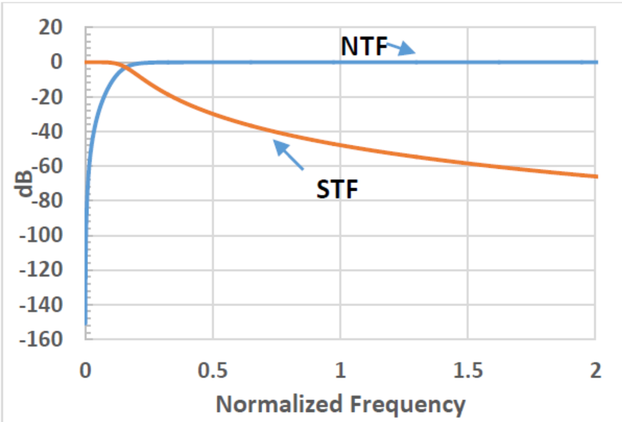

Fig.7. NTF and STF functions for the third-order proposed architecture.

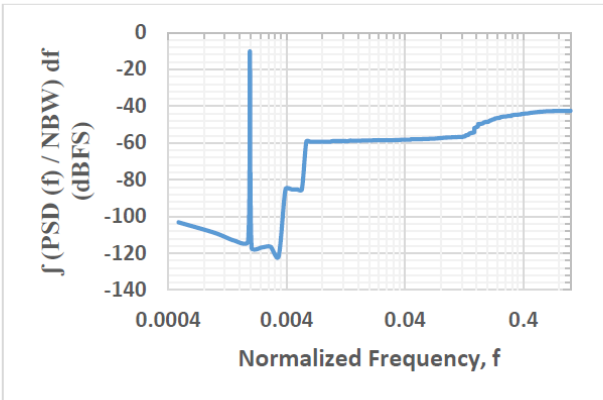

Fig.8. Simulated Integral version of PSD plot of second-order proposed modulator.

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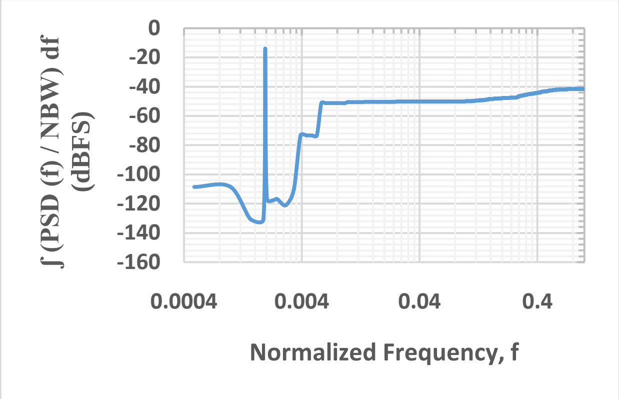

Fig.9. Simulated Integral version of PSD plot of third-order proposed modulator.

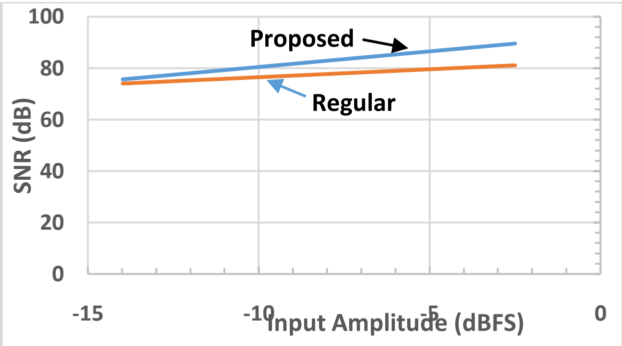

Fig.10. Simulated SNR plot of second-order modulator with input amplitude.

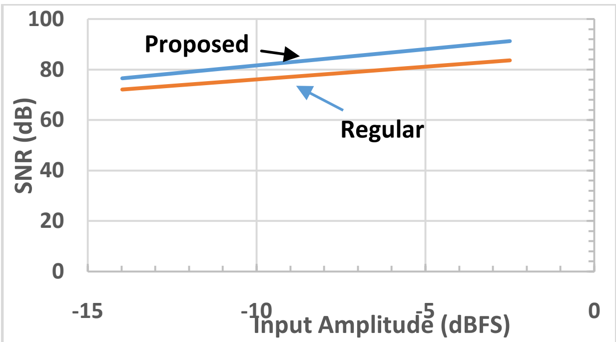

Fig.11. Simulated SNR plot of third-order modulator with input amplitude.

V. Conclusion

In this paper, a modified alternative architecture for the multiple- order single-bit quantizer based over-sampled DSMs was studied. The advantages gained from this architecture are higher speed, lesser static power dissipation and a slightly better SNR value. The drawbacks in this approach are the requirement of many pulses to get the required noise-shaping and mismatching error problem. The SPICE simulation for the second-order and third-order systems were studied using a typical design process and shown that the obtained SNR values are slightly better for the proposed architecture than that of the regular architecture.

References

[1] R.Schreier and G.C.Temes, “Understanding Delta-Sigma Data Converters”, IEEE Press, John Wiley & Sons Inc., 2005.

[2] S.R.Norsworthy, R.Schreier and G.C.Temes, “Delta-Sigma Data Converters”, IEEE Press, Piscataway NJ, 1997.

[3] David Johns and Ken Martin, “Analog Integrated Circuit Design”, John Wiley & Sons Inc., 1997.

[4] J.C.Candy and G.C.Temes,“Oversampling Methods for A/D and D/A Conversion”, IEEE press, New york, 1992.

[5] R.W.Adams et,all, “Theory and practical implementation of a fifth-order sigma-delta A/D converter”, J.Audio Eng.Soc., vol.39, pp.515-528, July 1991.

[6] D.R.Welland et.all. “Stereo 16-bit delta-sigma A/D converter for digital audio”, J.Audio Eng.Soc., vol.37, pp.476-486, June1989.

[7] P.F.Ferguson et.all,“One-bit higher-order sigma-delta A/D converters”, Proc.IEEE Int.Symp.Circuits Sys., vol.2, pp.890-893, May 1990.

[8] Y.Matsuya et.all,“A 16-bit Oversampling A-to-D Conversion Technology Using Triple–Integration Noise Shaping”, IEEE J.of Solid-State Circuits, vol.22, pp.921-929, Dec.1987.

[9] D.Anastassiou, “Error Diffusion Coding for A/D Conversion”, IEEE Trans. On Circuits and Systems, vol.36, pp.1175-1186, Sep.1989.

[10] C.C.Cutler,“Transmission systems employing quantization”, U.S.patent 2,927,962, filed 1954, issued 1960.

[11] P.Benabes et.all, “New wideband sigma-delta convertor”, IEE Electronic Letters, vol.29, no.17, pp.1575-1577, August 19, 1993.

[12] A.Yukawa, “A CMOS 8-bit High-Speed A/D Converter IC”, IEEE J.Solid-State Circuits, vol.SC-20, pp.775-779, June 1985.

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