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A Low Power Decoding Circuitry for a Multi Channel Data Acquisition System using Gate Diffusion Input

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Abstract — **Multichannel data acquisition systems require a decoding circuitry for selecting each channel and this paper describes such circuit with a new technique - Gate Diffusion Input. This technique makes the logic design less complex, consumes very low power reduces the propagation delay and also the area. A combinational circuit for implementing a 4 to 16 decoder is designed and implemented using GDI AND gate. Dynamic threshold is employed in the design and operates with a power supply of ± 0.4V. The total power consumption is reduced by switching the power and was measured around 3.2μW.**

Keywords — **Gate Diffusion, Low Power, Multichannel, Data Acquisition.**

I. INTRODUCTION

The demand for compact, high speed and portable digital applications together with low power dissipation has triggered various research efforts [1]-[3]. Many logic design techniques have been developed to improve the performance of Logic circuits built with traditional CMOS technology. One such technique most popular in low power digital circuits is the Pass Transistor logic (PTL).Various methods for implementing Pass Transistor Logic was implemented with nMOS where different control signals are applied to Gate and Source of the n-transistors. Numerous PTL technique implementations are reported in the literature [1],[2],[4]-[6] and [14].

PTL has several advantages over the conventional CMOS one being high speed because of low node capacitances, power dissipation is low because of less transistors and because of small area the interconnection effects are also low [7][8].

PTL implementations have certain disadvantages. In a single channel pass transistor the threshold drop reduces current drive and lowers the speed of operation at reduced supply voltages which is very important for low power design applications. Secondly the PMOS device in the inverter will not turn OFF fully resulting in direct path static power dissipation [4] and the 'high' input voltage at the regenerative inverters is not V_{DD}.

Variety of PTL circuits are evolved to solve the above mentioned disadvantages [5].

1) pMOS and nMOS transistors are combined to form a CMOS Transmission gate (TG) and various complex logic functions are realized using less number of complementary transistors. This solves the low logic level swing problem.

2) Combination of nMOS PTL with CMOS output inverters produces complimentary inputs/outputs called complementary pass transistor logic(CPL). The most important feature in this CPL logic is the small stack height and the low swing in the internal node thereby contributing low power consumption. Low swing at the gates of the output inverters introduces static power consumption.

3) To reduce the power consumption and to keep full swing operation complementary transistors are used and is called Double pass Logic (DPL). This suffers from large area because of the presence of pMOS transistors.

The capturing of major role in real logic LSIs is prevented by the pass transistors due to top down design complexity present in the existing PTL [6] because of non availability of simple and universal cell library in PTL based design.

This paper proposes a new Gate diffusion input technique that solves most of the problems mentioned above. Large range of complex logic functions can be implemented using only two transistors with GDI technique. Design of low power high speed circuits can be designed and implemented using less number of transistors compared to CMOS or PTL logic. The static power and logic level swing are improved with simple top down design using a small cell library.

II. BASIC FUNCTIONS OF GATE DIFFUSION INPUT

FIG(1) shows a simple cell of Gate Diffusion Input (GDI) method resembling a standard CMOS Inverter, however some differences exist.

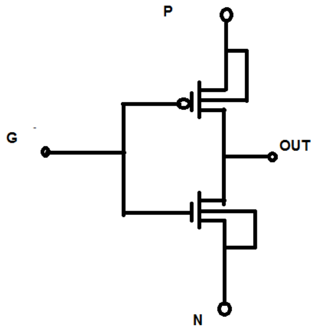

Fig1. GDI Cell

1) The cell contains three inputs: G (Input to the Gates of nMOS and pMOS), P(the Source/Drain input of pMOS) and N (Source/Drain input of nMOS).

2) Both the transistor bulks are connected to N or P respectively.

Various Boolean functions can be realized with a simple change of the input configuration of a GDI cell as given in Table 1.

Table 1: Boolean Functions of GDI cell

N	P	G	OUT	FUNC
‘0’	B	A	A^1B	F1
B	‘1’	A	$A^1 + B$	F2
‘1’	B	A	A + B	OR
B	‘0’	A	A.B	AND
C	B	A	$A^1B + AC$	MUX
‘0’	‘1’	A	A^1	NOT

Realizing the above functions in CMOS or PTL requires 6 to 12 transistors whereas the GDI technique requires only 2 transistors per function. In this AND gate is realized using GDI technique as shown in FIG2.

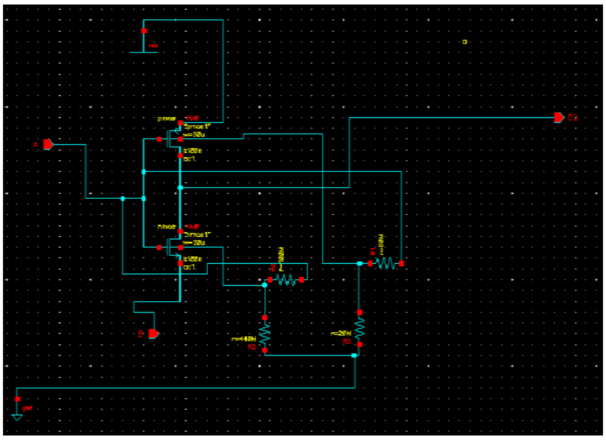

Fig.2. AND Gate Using GDI

The threshold voltage of the transistor increases when the body to source reverse bias is made larger, and decreases when the body to source is forward biased (less than 0.6V). This body bias technique is utilized in the dynamic threshold MOS transistor (DTMOS).

$$V_{th} = 2\Phi_B + V_{FB} + \frac{\left(2\varepsilon_s qN_a(2\Phi_B)^{1/2}\right)}{C_{OX}} \qquad (1)$$

As the voltage difference between the source and the bulk V_{SB} changes, the transistor threshold voltage V_t also changes. Since the threshold voltage V_t is effected by V_{SB}, this helps in identifying the transistor’s switching behavior. The expression for measuring the threshold voltage is given as

$$V_{th} = V_{Th0} + \gamma_B \; (|2\Phi_F + V_{SB}|)^{1/2} - |2\, \Phi_F|)^{1/2} \qquad (2)$$

Where γ_B (gamma) is the body coefficient, ϕ_F is the bulk Fermi- potential ,V_{Th0} is the threshold voltage when V_{SB}=0. The threshold voltage becomes dynamic when the V_{SB} is changed dynamically and the transistor is operated with dynamic threshold (DTMOS). The transistors performance can be improved by reducing the threshold voltage [10].

III. TRANSIENT ANALYSIS OF GDI CELL

The transient analysis of GDI cell and the standard CMOS inverter are almost identical and was presented in the literature [9][10]. The analysis is based on the Shockley model and the current I_D is expressed as :

$$I_D = \begin{cases} I_{D0}\,(W/L)\, e^{(qV_{GS}/KT)} \;; & (V_{GS} \le V_{TH} : \text{sub threshold region}) \\ K\{(V_{GS}-V_{TH})V_{DS} - 0.5V^2_{DS}\} & (V_{DS} < V_{GS} - V_{TH} : \text{linear region}) \\ 0.5K\,(V_{GS}-V_{TH})^2 \;; & (V_{DS} \ge V_{GS} - V_{TH} : \text{saturation region}) \end{cases} \qquad (3)$$

Where I_D is the Drain current, K is derivability factor, V_{TH} is threshold voltage, W and L are channel width and length.

In the analysis of CMOS inverter [8] V_{gs} is taken as input voltage but in most of the GDI circuits V_{ds} is considered as input voltage variable in the Shockley model.

When a step input is applied the nMOS transistor causes a drop in the output swing. During this time the nMOS transistor enters sub threshold region from saturation region. Due to the fast transition in the input the linear region can be omitted in the analysis. Considering the capacitive load at the output, the expressions for the transient response can be derived from (3). The capacitive current is given by

$$I_C = C\frac{dVs}{dt} = I_D \qquad (4)$$

Where I_D is the drain current through the nMOS transistor, C is the output capacitance, V_S is the voltage across the capacitance C_L, I_C is the current charging the capacitor.

In saturation region

$$C\,\frac{dVs}{dt} = 0.5k\,(V_{GS} - V_T)^2 = 0.5k\,(V_{DD} - V_T - V_S)^2 \qquad (5)$$

The integral form of (5) is

$$\int \frac{dVs}{0.5K(Vdd - Vt - Vs)^2} = \int \frac{dt}{C} \qquad (6)$$

The same expression can be written as

$$\int \frac{dVs}{aVs^2 + bVs + c} = \int dt \qquad (7)$$

$$a = 0.5k/C,$$

$$b = -k\,(V_{DD} - V_T) / C\,, \qquad (8)$$

$$c = 0.5k\,(V_{DD} - V_T)^2 / C$$

where a,b and c are constants of the process or the given circuit.

The two input GDI AND gate is combined to form a FOUR input AND gate with the fourth input acting as EN. The gate operates when the EN input is high. The schematic circuit of the Four input AND gate and the response is given in FIG 3 & 4 respectively.

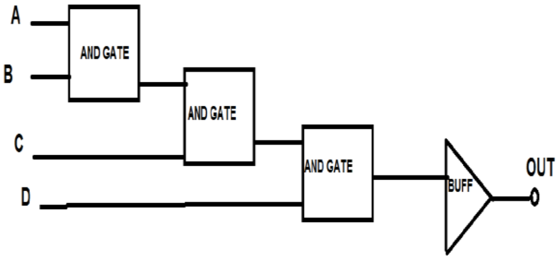

Fig.3. schematic diagram of FOUR input ANDgate

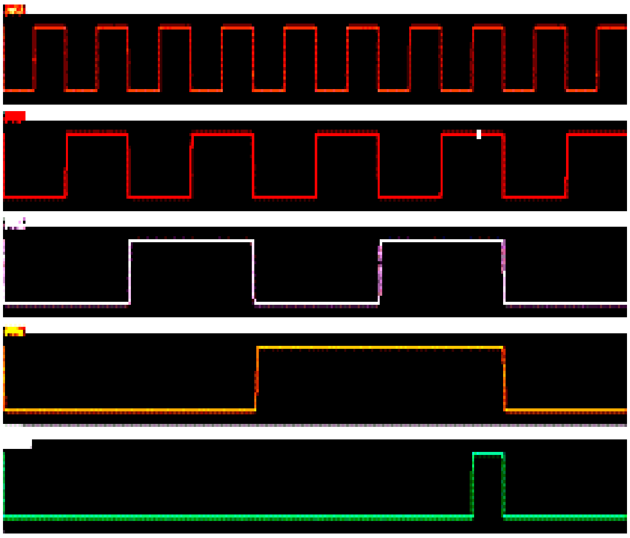

Fig.4. Response of GDI AND Gate

IV. DESIGN OF 4 TO 16 DECODER

The four input AND gate is used to design a 3 to 8 decoder with active eight HIGH outputs and three inputs. The fourth input is used as EN signal which will enable or disable the decoder. The circuit diagram and the response of the decoder is shown in the figures (5) and (6) respectively.

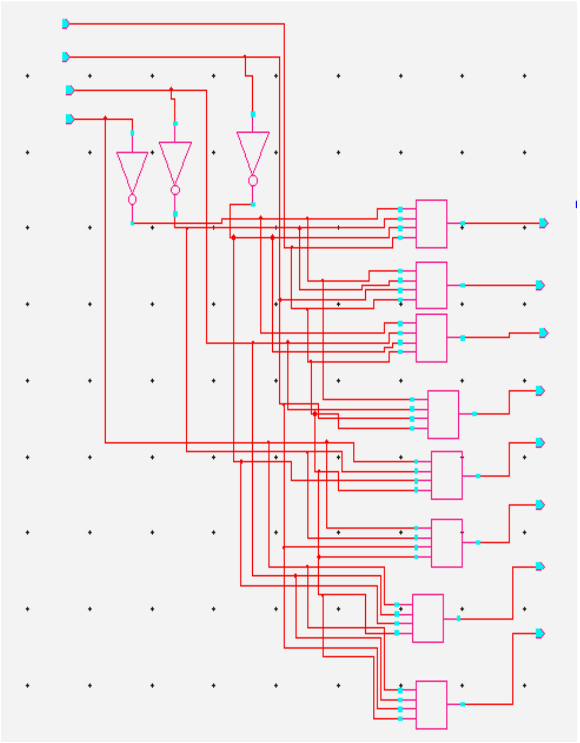

Fig.5. Schematic circuit of 3 to 8 decoder

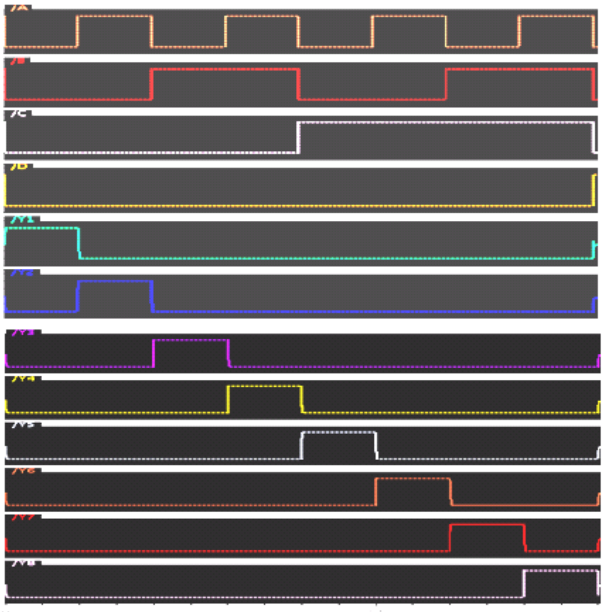

Fig.6. Response of 3 to 8 decoder when D input is ‘0’.

The 3 to 8 decoders are combined to form a 4 to 16 decoder is as sown in the FIG (7).

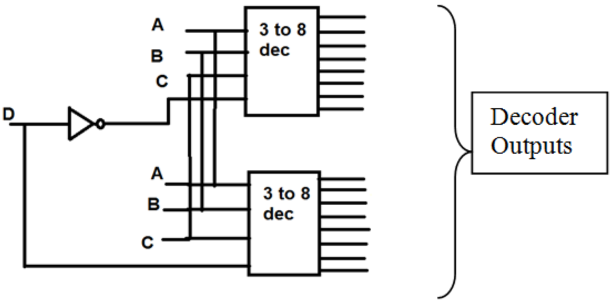

Fig.7. Block schematic of 4 to 16 decoder.

In order to reduce the power consumption the technique of switching power supply is employed wherein, when the D input (EN signal) is ‘LOW’ part of the switching circuit will turn ON to provide power i.e V_{dd} and V_{ss} to the first 3 to 8 decoder while the second decoder will be OFF. This will enable the decoder and the first eight outputs are obtained. When the D input goes ‘1’ the other part of the switching circuit will turn ON and provides power to the second decoder while the first one will be turned OFF. The other eight outputs were obtained. Since only one decoder gets the power supply at any point of time the power consumption is reduced by 50%. The transmission gate logic is used to design the switching circuitry for power supply.

V. TRANSMISSION GATE DESIGN

A transmission gate is used to implement analog switch that allows or blocks signals in a selected manner. Combination of PMOS and NMOS transistors are used to design a transmission gate which turns ON or OFF depending upon the control signal.

The circuit for a transmission gate is shown in FIG(8). An inverter is used to provide a complimentary signal to turn the transistors ON or OFF. When LOW the NMOS will get a ‘0’ and PMOS will get ‘1’ and both transistors are turned OFF. if the control signal is HIGH the NMOS will get ‘1’ and PMOS will get ‘0’ and both transistors were turned ON. However each transistor cannot conduct to both the power supply rails, but to either end by complimenting each other and together conduct to the rails.

The gate offers an infinite resistance in OFF condition theoretically but since there is always some conduction practically and so the resistance is finite in the order of few mega ohms. During ON condition the resistance of the gate should be very low typically in the order of few tens of ohms.

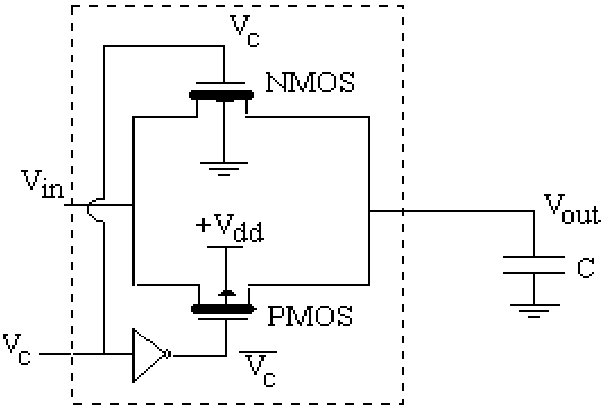

Fig.8. Transmission gate

The above gate is modified by stacking the transistors in order to ensure that there is no signal loss during transmission and stacking improves the aspect ratio, performance and ON resistance. The modified circuit is shown in Fig (9).

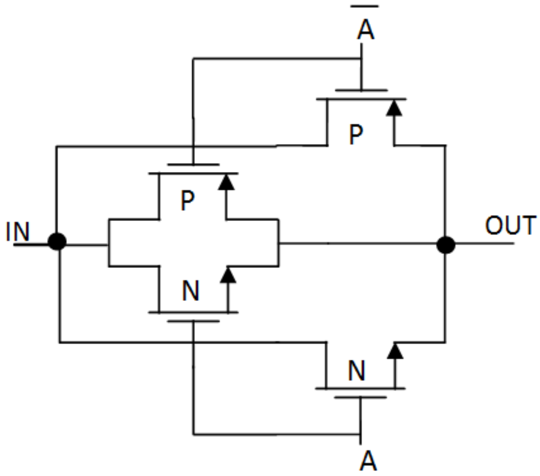

Fig.9. Modified transmission gate

The circuit for switching the power supplies using the above modified transmission gate is given in FIG 10.

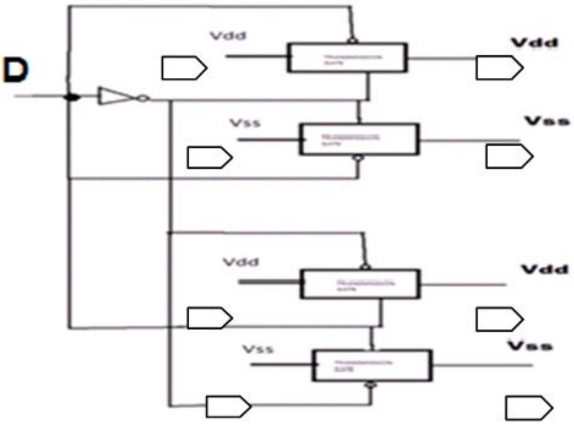

Fig.10. Transmission gate circuit for switching power supplies.

VI. CONCLUSION

A Gate Diffusion input technique for low power design was presented. A 4 to 16 decoder is designed and implemented using this technique. A 4 input AND gate was designed and the transistors are operated in sub threshold region by employing body biasing. The design was implemented in 180nm technology using CADENCE tools. To reduce the power consumption the power supplies were switched between the decoders. The switching circuitry is designed using the transmission gate logic. The total power consumption at a frequency of 1 KHz measured is 3.2 µW. The decoder can be used in applications like data acquisition systems, multiplexers etc.

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