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A Ring Oscillator Model and Design for a Self-biased CMOS PLL using Alpha-Power Law Based MOSFETs

Bhaskar Gopalan
Email: bhaskar_gopalan@hotmail.com

Abstract – **A simple modified design procedure for a Maneatis cell based ring oscillator without any elaborate bias generator suitable to self-biased CMOS PLL using alpha-power law based MOSFETs is presented. Also presented is the time-domain mathematical model for the simulation of voltage-controlled oscillator (VCO). The design shows how to fix the operating biasing current for VCO through a simple circuit. A closed-form solution for the model shows good agreement between the SPICE simulated design and the model. The VCO is simulated for a 0.13um, 1.2v process and the designed result shows the tuning range of the VCO vary from 190MHz to 540MHz. The maximum % Total harmonic distortion (%THD) obtained is 2% and the maximum power dissipated by the ring oscillator is 672µW. Also the maximum variation in oscillation frequency arising from low-frequency supply voltage noise is 7%. The proposed design also is compared with Maneatis cell based ring oscillator with bias generator and shown that proposed design without any elaborate bias generator is better in terms of supply voltage noise effect and %THD but poorer in terms of tuning range.**

Keywords – **Self-Biased CMOS PLL, VCO, SPICE Models, Alpha-Power Law Mosfets, VCO Tuning Range, Total Harmonic Distortion (THD), Power Dissipation And Supply Voltage Noise.**

I. Introduction

The rising demand for high-speed I/O has created an increasingly noisy environment in which PLL's must function. This noise, typically in the form of supply and substrate noise, tends to cause the output clock of PLL's to jitter from their ideal timing. Achieving low jitter in PLL designs can be difficult due to a number of design tradeoffs. The amount of input tracking jitter produced as a result of supply and substrate noise is directly related to how quickly the PLL can correct the output frequency, To reduce the jitter, the loop bandwidth should be set as high as possible. Unfortunately, the loop bandwidth is affected by many process technology factors and is constrained to be well below the lowest operating frequency for stability.

This paper considers a Maneatis cell based VCO for the PLL [1] which is based upon self-biased techniques. Self-biasing can remove virtually all of the process technology and environmental variability that plagues PLL designs. Self-biasing can provide a bandwidth that tracks the operating frequency. Other benefits include a fixed damping factor for the PLL's and input phase offset cancellation. Both the damping factor and the bandwidth to operating frequency ratio are determined completely by a ratio of capacitances giving effective process technology independence. By referencing most of all bias voltages and currents to other generated bias voltages and currents, the operating bias levels are essentially established by the operating frequency.

In this paper, a modified Maneatis VCO [1] without elaborate bias generator for the self-biased PLL using alpha-power law devices [2] is studied. A difference equation modeling of VCO is discussed in [3] and [6] whereas in this paper a mathematical modeling of VCO in closed-form expression has been obtained. A wide tuning range VCO is presented in [1] and [7]. The objective in this paper is to analyze and obtain a low-jitter VCO using alpha-power law devices against supply voltage noise and distortion.

This paper begins with a mathematical treatment for Maneatis cell based VCO model for a self-biased CMOS PLL in section II. Section III describes a simple modified design technique for Maneatis VCO. Also a supply voltage noise effect on VCO oscillation frequency is discussed in section III. Section IV concludes about the summary.

II. A Model for the VCO of a Self-Biased PLL

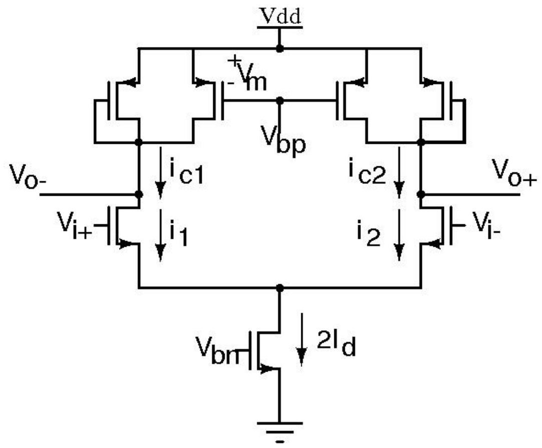

Fig.1. Differential VCO delay stage with symmetric loads (Maneatis cell) - (Reproduced from Ref. [1]).

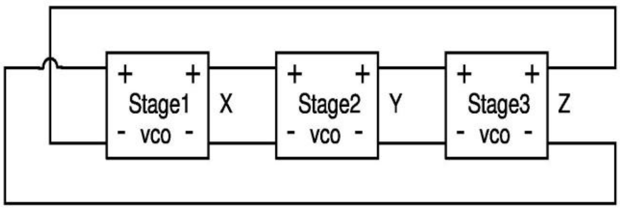

Fig.2 A three stage voltage controlled Ring Oscillator for the self-biased PLL [4].

A VCO circuit chosen for the PLL model [1] is shown in Fig.1 and Fig.2. It consists of a source-coupled differential pair (SCDP) with resistive load elements called symmetric loads. Symmetric loads consist of a

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diode-connected PMOS device in shunt with an equally sized biased PMOS device. The buffer delay changes with V_m since the effective resistance of the load elements also changes with V_m. These load elements lead to good control over delay and high dynamic supply noise rejection. The simple NMOS current source is biased with V_{bn}.

Let the currents i_1, i_2, i_{c1} and i_{c2} be as shown in Fig.2. Let x, y, z be the differential outputs of VCO for the three stages. $2I_d$ is the biasing current for all the three cells. Let the total linear capacitance at each output of the differential pair in the first stage be C and we can therefore write the equations at V_{o+} and V_{o-} as follows. The illustration below refers to the first cell and is well applicable for the other stages too.

$$C\frac{\partial V_{o+}}{\partial t}=i_{c2}-i_2 \qquad C\frac{\partial V_{o-}}{\partial t}=i_{c1}-i_1 \tag{1}$$

Let $V_{o+} - V_{o-} = x$, the differential output of the first stage of the VCO. Let Kn and Kp be the transconductance parameters of NMOS differential pair transistors and symmetric load PMOS transistors respectively. Let vtn and vtp be the threshold voltages of NMOS and PMOS transistors respectively and α and α_p be the alpha-power values of NMOS and PMOS transistors respectively. From (1), we have for the first cell using [2],

$$C\frac{\partial x}{\partial t}=(i_1-i_2)+(i_{c2}-i_{c1}) \tag{2}$$

Where,

$$i_{c2}-i_{c1}=-\left(\lambda_1 I_{d1}+\lambda_2 I_{d2}\right)x+P_m\left(x\right) \tag{3}$$

$$I_{d1}=\frac{Kp}{2}\left(V_m-|vtp|\right)^{\alpha_p} \tag{4}$$

$$I_{d2}=I_d-\frac{Kp}{2}\left(V_m-|vtp|\right)^{\alpha_p} \tag{5}$$

$$P_m\left(x\right)=\sqrt{\frac{\alpha_p}{2}}\left(\frac{Kp}{2I_{d2}}\right)^{\left(\frac{1}{\alpha_p}\right)}\left(2I_{d2}\right)(-x)\sqrt{1-\frac{\left(\alpha_p-1\right)Kp^{\left(2/\alpha_p\right)}}{4\left(2I_{d2}\right)^{\left(2/\alpha_p\right)}}x^2} \tag{6}$$

and

$$i_1-i_2 \approx G_m(-z)-\lambda_n I_d x \tag{7}$$

Where z = - (differential input voltage to the first cell). λ_1 and λ_2 are the channel length modulation parameters of top PMOS transistors of symmetric load respectively. I_{d1} and I_{d2} are the drain currents of these two transistors respectively and λ_n is the channel length modulation parameter of NMOS differential pair transistors.

$$G_m\left(z\right)=\sqrt{\frac{\alpha}{2}}Kn^{(1/\alpha)}\left(2I_d\right)^{(1-1/\alpha)}z\sqrt{1-\frac{\left(\alpha-1\right)Kn^{2/\alpha}}{4(2I_d)^{2/\alpha}}z^2} \tag{8}$$

The biasing current $2I_d$ varies with z for the first cell since

$$2I_d=2I_o+mz^2 \tag{9}$$

Where $2I_o$ is the input differential voltage independent biasing current.

The value of m needed to cancel out the higher degree dependency of $G_m(z)$ on z is given by [2],

$$m=\frac{\left(\alpha 2I_o/8\right)}{\left(2I_o/Kn\right)^{2/\alpha}} \tag{10}$$

Assuming that the higher degree dependency of G_m (-z) and P_m (x) have been cancelled out and assuming that,

$$\lambda_1 I_{d1}+\lambda_2 I_{d2} \approx \lambda I_o \tag{11}$$

Now, we have the equation (2) can be written as,

$$C\frac{\partial x}{\partial t}+\left[\left(\lambda+\lambda_n\right)I_o+P_m\right]x=-G_m z \tag{12}$$

Similarly for the other two cells or stages, we have,

$$C\frac{\partial y}{\partial t}+\left[\left(\lambda+\lambda_n\right)I_o+P_m\right]y=G_m x \tag{13}$$

$$C\frac{\partial z}{\partial t}+\left[\left(\lambda+\lambda_n\right)I_o+P_m\right]z=G_m y \tag{14}$$

The equations (12), (13) and (14) constitute the model for the three cells of the VCO. In (12), (13) and (14), G_m and P_m are given by (after neglecting higher order terms),

$$G_m=\sqrt{\frac{\alpha}{2}}\left(\frac{Kn}{2I_o}\right)^{1/\alpha}\left(2I_o\right) \tag{15}$$

$$P_m=\sqrt{\frac{\alpha_p}{2}}\left(\frac{Kp}{2I_{d2}}\right)^{1/\alpha}\left(2I_{d2}\right) \tag{16}$$

Now let us assume that x, y, z are given by,

$$x\left(t\right)\approx As+\left(A0-As\right)e^{-(t-tx0)/\tau} \qquad y\left(t\right)\approx As+\left(A0-As\right)e^{-(t-ty0)/\tau} \qquad z\left(t\right)\approx As+\left(A0-As\right)e^{-(t-tz0)/\tau} \tag{17}$$

Where As and A0 are steady-state and initial state values of the signals respectively and these are given for a rising exponential by As=A/2; A0=-A/2 and for a falling exponential by As=-A/2; A0=A/2, where (A/2) is the maximum amplitude of the signals x or y or z. The basic delay parameter τ using (12) is given by,

$$\tau=\frac{C}{P_m+\left(\lambda+\lambda_n\right)I_o} \tag{18}$$

Where P_m is given by (16) and C is the effective capacitance at either output of the each VCO cell.

Assuming that t = 0 and Substituting (17) in (12), (13) and (14), we obtain,

$$tz0=tx0=ty0=\tau\ \ln\left(\frac{2G_m}{G_m-P_m-\left(\lambda+\lambda_n\right)I_o}\right) \tag{19}$$

The frequency of oscillation is given by,

$$F_o=\frac{1}{2\left(tx0+ty0+tz0\right)} \tag{20}$$

From (17) and (12) we also obtain the maximum amplitude as given by,

$$\frac{A}{2}=\frac{I_{os}}{P_{ms}+P_1+\left(\lambda+\lambda_n\right)I_{os}} \quad (21)$$

Where P_1 is given by,

$$P_1=2\left(\frac{C}{\tau}-P_{ms}-\left(\lambda+\lambda_n\right)I_{os}\right)e^{\frac{tx0}{\tau}} \quad (22)$$

Where I_{os} is the bias current at the point when the bias current flows on only one of the two branches (i.e. i_1 or i_2 is zero / at the lower swing limit). P_{ms} is obtained using $2I_{d2s}$ in (16) where $2I_{d2s}$ is given by

$$2I_{d2s}=I_{os}-Kp\left(V_m-|vtp|\right)^{\alpha_p} \quad (23)$$

Having known all the parameter values in equation (17) and this completes the model for the VCO for a self-biased PLL based on alpha-power law devices.

III. The VCO Design

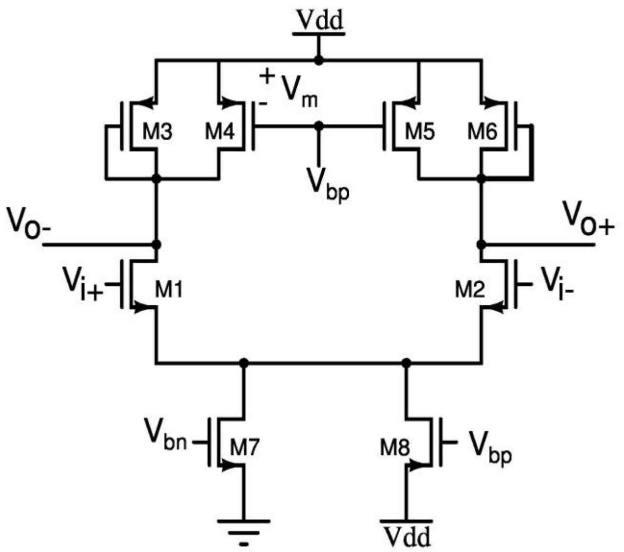

Fig.3. Modified VCO differential delay stage with PMOS transistor M8 in the biasing circuitry for biasing current fixation.

The complete VCO delay stage circuit based on model discussed in the above section is shown in Fig.3. It doesn't require any elaborate bias generator as in Ref. [1]. In Fig.3, V_m = vdd-V_{bp}. In the biasing circuitry, a NMOS transistor (M7) is biased with V_{bn} and an only extra element, a PMOS transistor (M8) is dynamically biased with V_{bp} as shown in Fig.3. A symmetrical PMOS transistors form the loads for the VCO delay stage. Biasing current ($2I_o$) =Current thro' M7-Current thro' M8.

The VCO cell delay changes with V_{bp} as the resistive load changes. In the biasing circuit, the PMOS transistor (M8) is driven by V_m. This gives good control over variation in the biasing current $2I_d$ with V_{bp} and also gives control over supply voltage noise. As the supply voltage increases or decreases slightly due to noise, the voltage at either outputs of delay stage increases or decreases and this changes the biasing current. This is approximately compensated by PMOS transistor (M8) current in the biasing circuit driven by V_m. Also the low transistor sizes of M1 and M2 make the higher degree dependency of G_m on x or y or z to be minimized, thus making differential current an approximately a linear as shown in equation (10).

The various parameters chosen for the self-biased PLL are given below. Some of these parameters are taken from BSIM3v3.1 SPICE Models of 0.13um, 1.2v, IBM CMOS process and the device sizes are taken from the design of VCO.

Supply voltage, Vdd = 1.2v.
epo = 8.8542e-12 F/m^2.
Dielectric constant of oxide layer (erox) = 4.0.
Oxide layer thickness (tox) = 4.1nm.
V_{bn} = 0.625v.
Kp = Kp_p(Wp/Lp) = 13.85e-06*(0.6u/0.15u) A/V^{α}.
Kn = Kn_n(Wn/Ln) = 40.0e-06*(10.0u/0.15u) A/V^{α}.
vtn = 0.366v.
vtp = -0.391v.
$\lambda = \lambda_n$ = 0.1/v.
α = 2.0.
α_p = 1.05 or 2.0.

It is noted that at lower currents of I_{d2}, the PMOS load transistor has an alpha-power value of 2.0 whereas at moderately higher currents, it has an alpha-power value of 1.05. Also it is noted that Kp and α_p in equation (23) show different values as different from the above mentioned due to low currents and are given by,
Kp = Kp_p(Wp/Lp) = 4.0e-06*(0.6u/0.15u) A/V^{α}.
α_p = 1.5 or 2.0.
The capacitance C is obtained from,

C_1=(2.0/3.0)*(epo*erox/tox)*(WnLn+WpLp)=9.15f.
C = C_1+Cgd,n+Cgd,p+2Cbd,p+Cbd,n = 15fF.

The SPICE simulated waveforms for the differential outputs of three differential stages for vdd=1.2v and V_{bp}=0.6v are shown in Fig.4. The VCO output frequency in Fig.4 is 500MHz.

The various simulated and estimated parameters including frequency of oscillation for different V_{bp} are tabulated in Table.I. The Table.I lists the values for VCO frequency obtained using SPICE simulated design and the model discussed in section II. It also shows that bias current $2I_o$ is approximately a constant one.

The maximum amplitudes of the signals for different V_{bp} are tabulated in Table.II. This table shows the amplitude of the signals obtained using SPICE simulated design and the proposed model as described in section II. A simple level-shifter may be used at the outputs of VCO to convert the differential signals into single-ended rail-rail voltages.

The changes in the frequency of oscillation and the maximum amplitude of the signals between SPICE simulation and the proposed model (as noticed in Table.I and II) are due to the variations in the device parameters namely KP_n, KP_p, vtn, vtp, α, α_p, λ_n and λ with respect to their bias values.

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Table.III shows %Total harmonic distortion (%THD) and the power dissipated by VCO (in µW) for different control voltage. The power dissipation varies with respect to V_{bp} due to the presence of transistor (M8) in delay stage circuit as in Fig.3.

The variation in VCO frequency for a low-frequency square wave supply voltage noise is also studied. The amplitude of the noise is chosen as +/-2.5% of vdd. For vdd=1.23v and V_{bp}=0.6v, the SPICE simulated values are $2I_o$=37uA and F_o=535MHz (a change of 7%). Similarly for vdd=1.17v and V_{bp}=0.6v, the SPICE simulated values are $2I_o$=25uA and F_o=465MHz (a change of 7%).

It is simulated and studied that the effect of supply voltage noise is more in Maneatis cell based VCO (with elaborate bias generator as in Ref. [1]) than the present proposed design and the change in oscillation frequency for a typical case is more than 10% in the former case. Also the %THD is approximately twice in Maneatis VCO with bias generator than the proposed design. But the tuning range is much larger in the former case (583MHz) than the proposed design (350MHz).

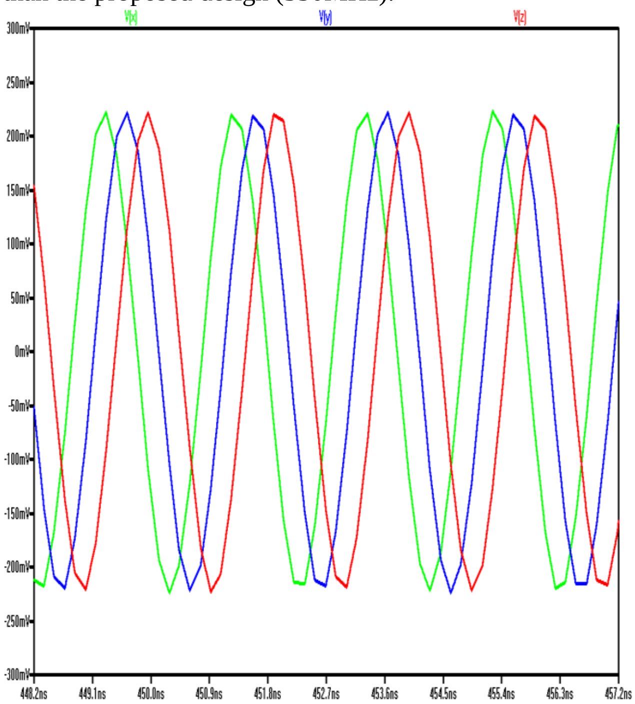

Fig.4 SPICE Simulated waveforms of VCO outputs v(x), v(y) and v(z) for the three differential stages. Vdd=1.2v and V_{bp}=0.60v. The VCO output frequency is 500MHz.

Table I: The VCO Frequency Results

V_{bp} volts)	$2I_o$ (uA)	$2I_{d2}$ (uA)	VCO F_o (MHz)	
			Design (Simulated)	Model (SectionII)
0.45	24.0	2.90	194.2	222.0
0.50	32.0	12.93	365.1	415.4
0.55	33.0	16.60	453.3	459.0
0.60	34.0	20.20	499.0	497.0
0.65	27.5	23.60	522.7	534.4
0.70	28.0	24.80	533.6	536.8
0.75	28.4	25.60	538.5	538.6
0.80	28.7	26.10	538.6	539.9

Table II: The Results of Maximum Amplitude of signals

V_{bp} (volts)	$2I_o$ (uA)	I_{os} (uA)	Maximum Amplitude, A/2 (in mv)	
			Design (Simulated)	Model (Section II)
0.45	24.0	12.0	607	578
0.50	32.0	20.0	366	316
0.55	33.0	20.66	282	259
0.60	34.0	20.70	220	220
0.65	27.5	20.75	180	166
0.70	28.0	20.73	160	165
0.75	28.4	20.19	152	159
0.80	28.7	20.53	148	162

Table III: Simulated Results of % Total harmonic distortion and Power dissipation.

V_{bp} (volts)	F_o (MHz) (Simulated)	%THD (Simulated)	Power Dissipation in µW (Simulated)
0.45	194.2	1.84	672
0.50	365.1	1.67	500
0.55	453.3	2.06	328
0.60	499.0	1.59	205
0.65	522.7	1.64	138
0.70	533.6	2.07	109
0.75	538.5	1.51	99
0.80	538.6	1.93	95

IV. Conclusion

A simple modified design of Maneatis cell based Ring oscillator without any elaborate bias generator suitable to a self-biased CMOS PLL using alpha-power law devices was discussed. The design includes fixing of the biasing current corresponding to variation in the control voltage. Also an approximate mathematical model for the same ring oscillator has been presented. The designed SPICE results show close agreement between the SPICE and the model results. The results of oscillation frequency, amplitude of the signals, power dissipation and the %Total harmonic distortion were studied. The variation in oscillation frequency due to low-frequency supply voltage noise was also studied and the results were given. Also the results for the Maneatis cell based ring oscillator with bias generator and the proposed modified design were compared.

References

[1] John G. Maneatis , "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE J. of Solid-State Circuits, vol.31, No.11, pp.1723-1732, Nov.1996.

[2] Bhaskar Gopalan, "Design of Linear CMOS Transconductance Elements for Alpha-Power Law based MOSFETs and an Automatic Compensation Technique for Temperature", Universal Journal of Electrical and Electronic Engineering, Horizon Research Publishing, USA, Vol.2, no.5, pp.234-244, 2014.

[3] David Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley & Sons, Inc., 1997.

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Volume 6, Issue 3, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

[4] Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, Inc., 2001.
[5] R.Best, Phase-locked loops, McGraw-Hill,1993.
[6] Monolithic Phase-Locked Loops and Clock Recovery Circuits: Theory and Design, Edited by Behzad Razavi, IEEE Press, 1996.
[7] I. Young et.1l., “A PLL clock generator with 5 to 110MHz of lock range for microprocessors”, IEEE J.Solid State Circuits, vol.27, no.11, pp.1599-1607, Nov.1992.

AUTHOR’S PROFILE

Bhaskar Gopalan
was born in Salem, Tamilnadu, India in 1966. He received the B.E degree in electrical engineering from PSG college of Technology, Coimbatore, India and the M.Tech. degree in electrical engineering from Indian Institute of Technology, Kanpur, India in 1987 and 1989 respectively.
He worked at many companies including ITI, Intergraph, WIPRO in India and Infineon Technologies Asia Pacific in Singapore. Currently he is an independent Technical Consultant in India. His research interests include low-power Analog/Mixed-signal/RF/Digital IC design and EDA work.