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Congestion and Power Reduction by using Merged Flip Flops

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***Abstract* – This paper presents Integrated circuit design process. In IC design process it has different steps like Floor plan, Power plan, Placement, Clock tree Synthesis and Routing. It must have a relation in between each and every process. Among these it has a significant relation in between clock and power consumption. The power consumption of IC can be depending on clock toggles. By replacing of few single bit Flip flops by multi-bit Flip flops it can reduces power. By merging of Flip flops it reduces congestion and area of the design. This design can reduce power by approximately 30%. Congestion plays a major role in VLSI circuits. This design optimizes congestion to the accurate level. And it meets the perfect timing. In order to meet the timing it should meet setup as well as hold.**

***Keywords* – Clock Toggle, Power consumption, Multi-bit Flip flops, Congestion.**

I. INTRODUCTION

In modern days the small designs are attracting the entire world due to portability, high speed, low power and reliability. As day by day technology developing that means the component count may double. As component count increases in IC that leads to high power consumption and clock speed also increases. These are the major factors to get power consumption. So, by improving of technology the power consumption is a biggest challenge for designer. The power consumption of IC can be divided into two that are static power and dynamic power consumption. The static power dissipation also called leakage of SOC. Dynamic power consumption can have both external and internal capacity loads also high toggle rate of clock.

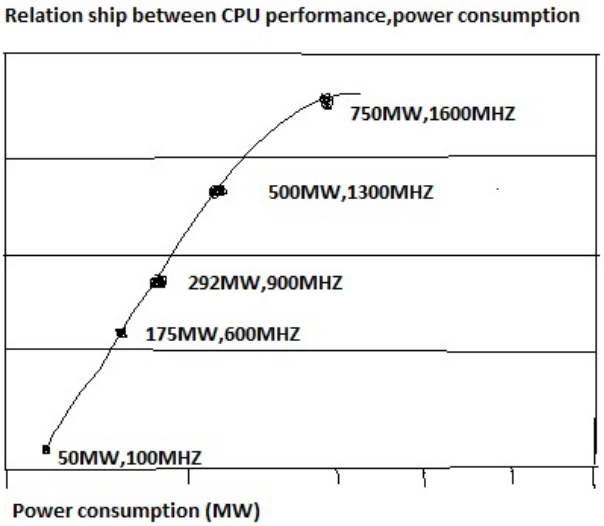

Fig.1. Power consumption Vs Clock frequency

The relation between power and the clock frequency

$P = f*c*v^{2,}$ where c is a capacitance.

In low power VLSI has several techniques to reduce power consumption are low power placement, gate level power optimization, and multi-bit flipflops.

II. DESIGN PROCESS

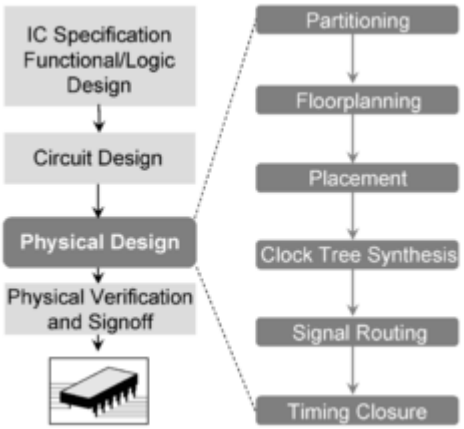

Fig.2. Flow of physical design

In physical design before clock tree synthesis it has optimization process that is called as post placement technique. In general placement process it place standard cells on core area of IC. After placing the standard cells it can check possibility of optimization. It identifies single bit Flip flops.

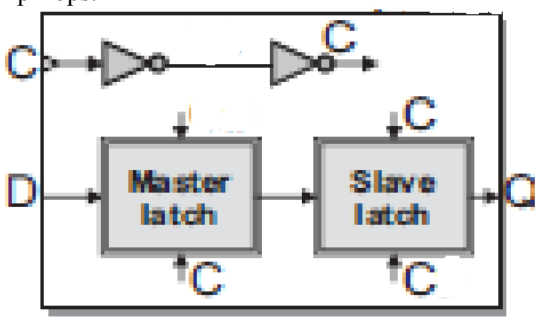

Fig.3. Single bit Flip-Flop

By identifying single bit flip flop and by removing two single bit flip flops by multi bit flip flop. By this process the clock count may reduces. Due to that clock toggle rate minimizes in the power consumption can also reduces. Portable multimedia and communication devices have experienced explosive growth recently. Longer batter life is one of the crucial factors in the widespread success of these products. As such, low-power circuit design for

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multimedia and wireless communication applications has become very important. In many such products, multi-bit flipflops and delay buffers (line buffers, delay lines) make up a significant portion of their circuits [1]–[3]. Such serial access memory is needed in temporary storage of signals that are being processed, e.g., delay of one line of video signals, delay of signals within a fast Fourier transform (FFT) architectures [4], and delay of signals in a delay correlator [2].

III MULTI BIT FLIP-FLOP

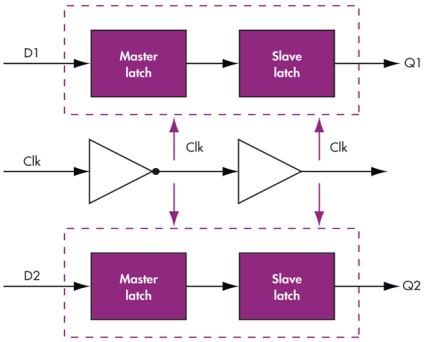

Fig.4. Multi bit flip-flop.

If any timing violations are occur that can resolve by placing inverters/buffers. This process follows a logical hierarchy method to connect clock roots to sinks of flip fops. Due to the manufacturing rules, inverters in flip-flops tend to be oversized. As the process technology advances into smaller geometry nodes like 65nm and beyond, the minimum size of clock drivers can drive more than one flip-flop. Merging single-bit flip-flops into one multi-bit flip-flop can avoid duplicate inverters, and lower the total clock dynamic power consumption. The total area contributing to flip-flops can be reduced as well. By using multi-bit flip-flop to implement ASIC design, users can enjoy the following benefits:

- ✓ Lower power consumption by the clock in sequential banked components
- ✓ Smaller area and delay, due to shared transistors and optimized transistor-level layout.
- ✓ Reduced clock skew in sequential gates

Begin-clock-tree 4
Clock-net-core/clock
Buffer-level buf*4
Buffer-level inv * 8
Buffer-level buf *8
Buffer-level inv * 8
End-clock-tree

This method reduces latency and improves positive slack. These both are good for setuptime.

Save flip flop power and area

Bit number	1	2	4
Power per bit	1.000	0.860	0.780
Area per bit	1.000	0.960	0.713

However after the replacement some flip flops would change and wire length of net connected flip flops also changes. To avoid this violation we restrict that wire length connected to flip flop cannot be longer after this process. A new flip flop can join beside this region and also consider the capacity of that region. As shown in figure after the two 1-bit flip flops f1 and f2 replaced with 2-bit flip flops. The wire lengths of net1, net2, net3 are changed. To avoid this violation nets values cannot be longer than specified values. We divide the total placement region into several bins. Each bin has a certain capacity and remaining area can be placed by additional cells.

Suppose the area of f3 is 7, f3 is already assigned to f1. We cannot place in f3 bin because the area is smaller. And we also check whether the cell library provides flip flop information or not? We have to check the availability of 2-flip flop. We replace 1-flip flop by 2-flip flop.

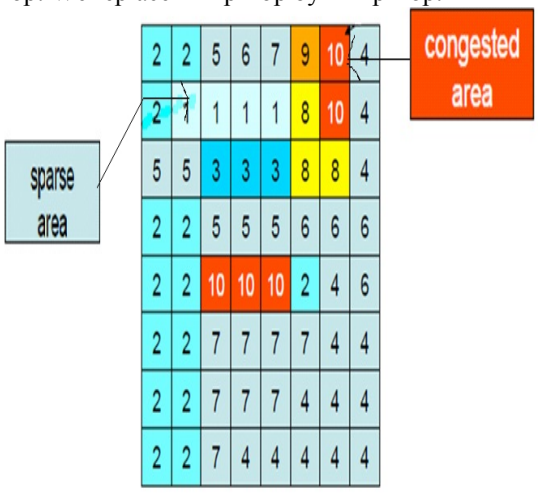

Fig 5.0

Algorithm

Algorithm INTEGRA
// Initialization
1. lexicographically sort the MBFF library
2. collapse MBFFs
3. $X' \leftarrow$ sort $\{s_x(i), e_x(i): i = 1..n\}, j \leftarrow 1, Q \leftarrow \varnothing$
// Main body
4. **while** (X' is not empty) **do**
5. find a decision point in X'
6. $Q \leftarrow Q +$ essential flip-flops and related flip-flops
7. $Y' \leftarrow$ sort $\{s_y(i), e_y(i): i \in Q\}$
8. **foreach** essential flip-flop k **do**
// Flip-flop clustering
9. $K_{max} \leftarrow$ max_clique(Y', k)
10. find the appropriate MBFF cell of bit number B for $|K_{max}|$
11. $K_{max} \leftarrow$ sort $\{e_x(i): i \in K_{max} - \{k\}\}$
12. $K_j \leftarrow$ flip-flop k and the first (B-1) flip-flops in K_{max}
// Flip-flop placement
13. find bounding box B_b for K_j
14. project B_b's corner and center points to $F_r(K_j)$
15. find the projected point with min distance between B_b and $F_r(K_j)$
16. legalize this point and assign it to MBFF K_j
17. if legalization fails **then** go to line 9
18. $Q \leftarrow Q - K_j, X' \leftarrow X' - K_j$
19. j++

Now we can see the algorithm for combinational logic. In that it starts from checking which flip flops are nearer in subdivisions of the chip. Here we can check single bit flip

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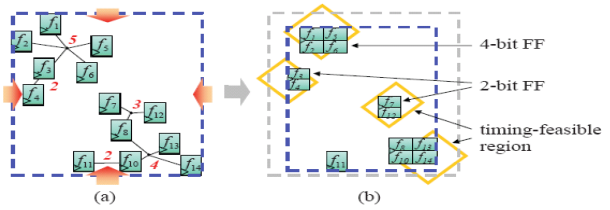
flops. If it is nearer we can combine it and form a 2-bit or 3-bit flip flops .Means after selection merging of flip-flops would done. The process repeats until all the flip flops would be merge.



Rout ability optimization is a major concern in modern day technologies. Interconnect has become a major factor of all over performance of a circuit. In order to reduce the interconnect cost we need a good congestion estimation method. When locations of the packings are very congested the nets would be detour. We have preliminary estimation and detailed estimation. We estimate the congestion measure at each tile according of each net so that we determine which regions are to be over congested. In detailed estimation based on preliminary estimation of each net by using diagonal congestion model. Finally congestion redistribution, in this process by moving wires from over congested to lesser congestion.

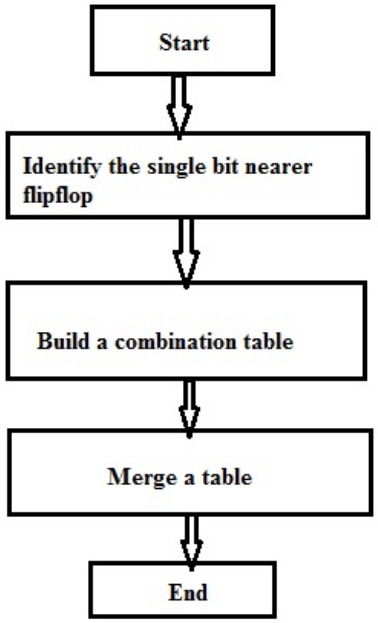
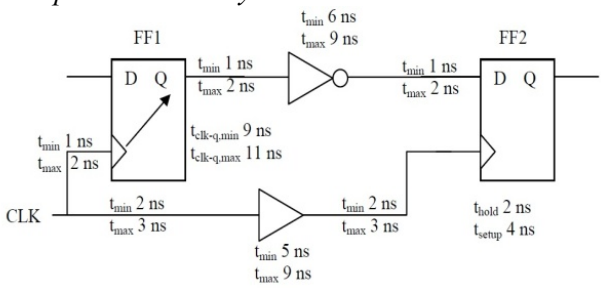


Fig.6.0 Algorithm for combinational logic

IV. Timing Analysis

A Setup and hold analysis



When a hold check is performed, we have to consider two things-

- Minimum Delay along the data path.
- Maximum Delay along the clock path.

If the difference between the data path and the clock path is negative, then a timing violation has occurred. (Note: there are few Exceptions for this- We will discuss that some other time)

Data path is: CLK->FF1/CLK ->FF1/Q ->Inverter ->FF2/D

Delay in Data path= min(wire delay to the clock input of FF1) + min(Clk-to-Q delay of FF1) +min(cell delay of inverter) + min(2 wire delay- "Qof FF1-to-inverter" and "inverter-to-D of FF2")=Td = 1+9+6+(1+1)=18ns

Clock path is: CLK-> buffer -> FF2/CLK

Clock path Delay= max(wire delay from CLK to Buffer input) + max(cell delay of Buffer) + max(wire delay from Buffer output to FF2/CLK pin) + (hold time of FF2)=Tclk = 3+9+3+2 = 17 ns

Hold Slack = Td - Tclk = 18ns -17ns = 1ns

Since Hold Slack is positive-> No hold Violation**.**

When a setup check is performed, we have to consider two things-

- Maximum Delay along the data path.
- Minimum Delay along the clock path.

If the difference between the clock path and the data path is negative, then a timing violation has occurred. (Note: there are few Exceptions for this- We will discuss that some other time)

Data path is: CLK->FF1/CLK ->FF1/Q ->Inverter ->FF2/D

Delay in Data path= max(wire delay to the clock input of FF1) + max(Clk-to-Q delay of FF1) +max(cell delay of inverter) + max(2 wire delay- "Qof FF1-to-inverter" and "inverter-to-D of FF2")**=Td = 2+11+9+(2+2) = 26ns**

Clock path is: CLK-> buffer -> FF2/CLK

Clock path Delay= (Clock period) + min(wire delay from CLK to Buffer input) + min(cell delay of Buffer) + min(wire delay from Buffer output to FF2/CLK pin) - (Setup time of FF2)=Tclk = 15+2+5+2-4=20ns

Setup Slack = Tclk - Td = 20ns - 26ns = -6ns.

Since Setup Slack is negative -> Setup violation.

V. Conclusion

This paper presentd Integrated circuit design process. The power consumption of IC can be depended on clock toggles. By replacing of few single bit Flip flops by multi-bit flip flops it reduces power. By merging of Flip flops it reduced congestion and area of the design. This design reduced power by approximately 30%.It can improve slack of flip flop and also it is better for setuptime and its better for congestion analysis. In order to meet the criteria of the design major considerations are timing, area, congestion, power. This design have designed by consideration of all factors.

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AUTHOR'S PROFILE

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