

Enhancement of Power Quality by CSC-UPQC using Fuzzy Logic Technique

Ch. Suresh Kumar

M.Tech., Department of EEE
 St. Theresa Engineering College
 Vizag- 530 045, AP, India
 Email: sureshipl@gmail.com

G. Shiva Ram Prasad

Testing Engineer-Validation Department
 Kernex Microsystems (I) Ltd.
 Hyderabad-500045, India
 Email: shivaram.gummadi@gmail.com

B. Shankar Prasad

Head of the Department – EEE
 St. Theresa Engineering College
 Vizag- 530 045, AP, India
 Email: bshankarprasad@gmail.com

Abstract – This paper presents a new unified power-quality conditioning system - UPQC), capable of simultaneous compensation for voltage and current in multibus/multifeeder systems for three-phase unified power quality conditioner based on current source converters(CSC - UPQC), including the design guidelines of the key components, an appropriate control scheme, and a selection procedure of the dc current level. Particularly, the ride through capability criterion is used to define a minimum dc current level so that the CSC-UPQC with Fuzzy technique achieves the same characteristics as a UPQC based on current-source converters in terms of voltage disturbance compensation in the point of common coupling (PCC) and load power factor compensation. A 1.17 MVA load fed from a 3.3 kV system is used to show the proposed design procedure, and a laboratory prototype is implemented to show the system compensating Harmonics, interruptions, sags and swells using low switching frequency in the CSC and maintaining a unitary displacement power factor in the PCC with ANN technique.

Keywords – Artificial Neural Networks (ANN), Current Source Converters, Nonlinear Control, Power Quality (PQ), Unified Power-Quality Conditioner (UPQC).

I. INTRODUCTION

With increasing applications of nonlinear and electronically switched devices in distribution systems and industries, power-quality (PQ) problems, such as harmonics, flicker, and imbalance have become serious concerns. In addition, lightning strikes on transmission lines, switching of capacitor banks, and various network faults can also cause PQ problems, such as transients, voltage sag/swell, and interruption. On the other hand, an increase of sensitive loads involving digital electronics and complex process controllers requires a pure sinusoidal supply voltage for proper load operation [1].

In order to meet PQ standard limits, it may be necessary to include some sort of compensation. Modern solutions can be found in the form of active rectification on a active filtering [2]. A shunt active power filter is suitable for the suppression of negative load influence on the supply network, but if there are supply voltage imperfections, a series active power filter may be needed to provide full compensation [3].

In recent years, solutions based on flexible ac transmission systems (FACTS) have appeared. The application of FACTS concepts in distribution system has resulted in a new generation of compensating devices. A Unified Power-Quality Conditioner (UPQC) [4] is the extension of the unified power-flow controller (UPFC) [5]

concept at the distribution level. It consists of combined series and shunt converters for simultaneous compensation of voltage and current imperfections in a supply Feeder [6]-[8]. Recently, multiconverter (FACTS) devices, such as Interline Power-Flow Controller (IPFC) [9] and the Generalized Unified Power-Flow Controller (GUPFC) [10] are introduced. The aim of these devices is to control the power flow of multilines.

When the power flows from two lines starting in one substation need to be controlled, An IPFC consists of two series CSCs whose dc capacitors are coupled. This allows active power to circulate between the CSCs. With this configuration, two lines can be controlled simultaneously to optimize the network utilization.

This concept can be extended to design multi-converter configurations for PQ improvement in adjacent feeders. For example, the Interline Unified Power-Quality Conditioner (IUPQC), which is the extension of the IPFC concept at the distribution level, has been proposed in [11]. The IUPQC consists of one series and one shunt converter. It is connected between two feeders to regulate the bus voltage of one of the feeders, while regulating the voltage across a sensitive load in the other feeder. In this configuration, the voltage regulation in one of the feeders is performed by the shunt-CSC. However, since the source impedance is very low, a high amount of current would be needed to boost bus voltage in case of a voltage sag/swell which is not feasible. It also has low dynamic performance because the dc-link capacitor voltage is not regulated.

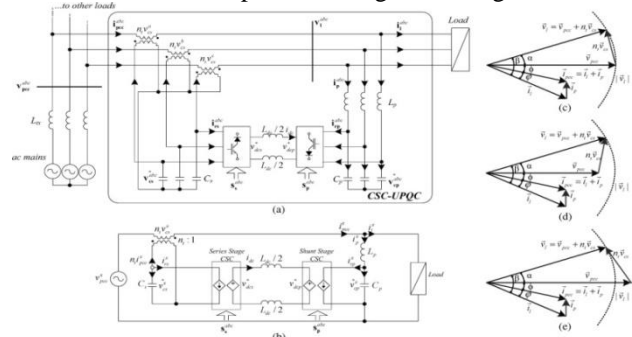


Fig.1. Block Diagram of CSC-UPQC

In this paper, a new configuration of a UPQC called the multi-converter Unified Power Quality Conditioner (CSC_UPQC) is presented. The system is extended by adding a series CSC in an adjacent feeder. The proposed topology can be used for Simultaneous compensation of voltage and current imperfections both feeders by sharing power compensation capabilities between two adjacent feeders which are not connected. The system is also

capable of compensating for interruptions without the need for a battery storage system and consequently without storage capacity limitations. The performance of the CSC-UPQC as well as the adopted control algorithm is illustrated by simulation. The present work study the compensation principle and different control strategies used here are based on PI & ANN Controller of the CSC-UPQC in detail. The results obtained in MATLAB/PSCAD on two-bus/two-feeder system shows the effectiveness of the proposed configuration.

II. PROPOSED CSC-UPQC SYSTEM

A. Circuit configuration

The single-line diagram of a distribution system with a CSC-UPQC as shown in Fig. 1. In this figure two feeders connected to two different substations supply the loads L1 and L2 With STATCOM. The CSC-UPQC is connected to two buses BUS1 and BUS2 with voltages of u_{t1} and u_{t2} respectively. The shunt part of the CSC-UPQC is also connected to load L1 with a current of i_{l1} . Supply voltages are denoted by u_{s1} and u_{s2} while load voltages are denoted by u_{l1} and u_{l2} . Finally, feeder currents are denoted by i_{s1} and i_{s2} and load currents are i_{l1} and i_{l2} .

Bus voltages u_{t1} and u_{t2} are distorted and may be subjected to sag/swell. The load L1 is a nonlinear/sensitive load which needs a pure sinusoidal voltage for proper operation while its current is no sinusoidal and contains harmonics. The load L2 is a sensitive/critical load which needs a purely sinusoidal voltage and must be fully protected against distortion, sag/swell and interruption. These types of loads primarily include production industries and critical service providers, such as medical centers, airports, where voltage interruption can result in service economical losses or human damages.

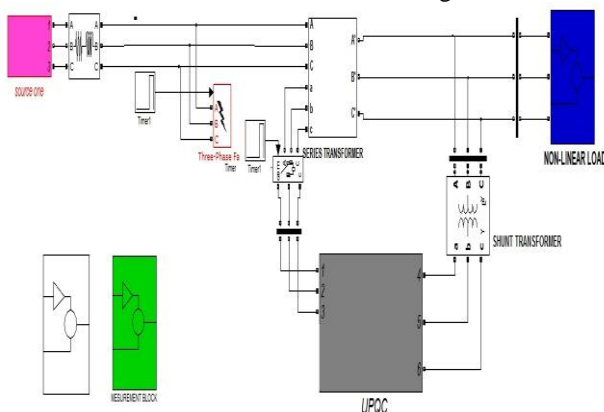


Fig.2. Typical Sim-link Block diagram CSC-UPQC used in distribution system.

B. CSC-UPQC Structure

The internal structure of the CSC-UPQC is shown in Fig. 2. It consists of three CSCs (CSC1, CSC2, and CSC3) which are connected back to back through a common dc-link capacitor. In the proposed configuration, CSC1 is connected in series with BUS1 and CSC2 is connected in parallel with load L1 at the end of Feeder1. CSC3 is connected in series with BUS2 at the Feeder2 and each of

the three CSCs in Fig. 2 is realized by a three-phase converter with a commutation reactor and high-pass output filter as shown in Fig. 3. The commutation reactor (L_f) and high-pass output filter (R_f, C_f) are connected to prevent the flow of switching harmonics into the power supply. As shown in

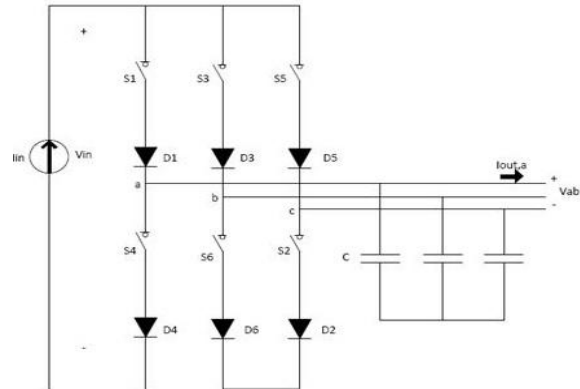


Fig.3. Current Source Converter (CSC) Schematic Diagram.

Fig. 2, all converters are supplied from a common dc-link capacitor and connected to the distribution system through transformer. Secondary (Distribution) sides of the series-connected transformers are directly connected in series with BUS1 and BUS2, and the secondary (distribution) side of the shunt-connected transformer is connected in parallel with load L1. The main aims of CSC-UPQC shown in Fig. 2 are:

- 1) To regulate the load voltage (u_{l1}) against sag/swell and disturbances in the system to protect the nonlinear/sensitive load L1;
- 2) To regulate the load voltage (u_{l2}) against sag/swell, interruption and disturbances in the system to protect the sensitive/critical load L2;
- 3) To compensate for the reactive and harmonic components of nonlinear load current (i_{l1})

In order to achieve these goals, series CSCs (i.e., CSC1 and CSC3) operate as voltage controllers while the shunt CSC (i.e., CSC2) operates as a current controller.

C. Control Strategy

As shown in Fig. 2, the CSC-UPQC consists of two series CSCs and one shunt CSC which are controlled independently. The switching control strategy for series CSC's and the shunt CSC's are selected to be sinusoidal Pulse width-modulation (SPWM) voltage control and hysteresis current control, respectively. Details of the control algorithm, which are based on the $d-q$ method [12], will be discussed later.

Shunt-CSC: functions of the shunt-CSC are:

- 1) To compensate for the reactive component of the load L1 current;
- 2) To compensate for the harmonic components of the load current;
- 3) To regulate the voltage of the common dc-link capacitor.

The measured load current ($i_{l_{abc}}$) is transformed into the synchronous $dq0$ reference frame by using

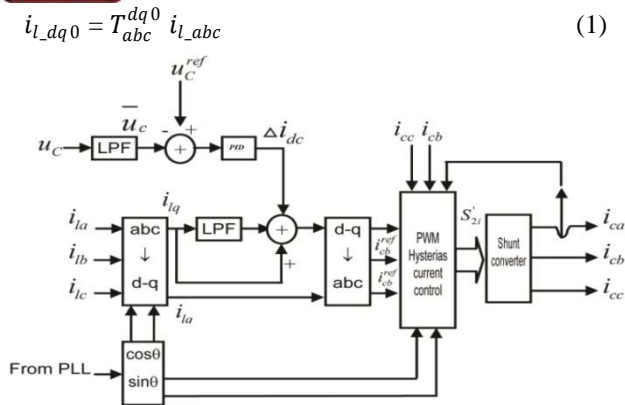


Fig. 4 represents the control block diagram for the shunt CSC.

Where, the transformation matrix is shown in (2).

$$T_{abc}^{dq0} = \frac{2}{3} \begin{bmatrix} \cos(\omega t) & \cos(\omega t - 120^\circ) & \cos(\omega t + 120^\circ) \\ -\sin(\omega t) & -\sin(\omega t - 120^\circ) & -\sin(\omega t + 120^\circ) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (2)$$

By this transformation, the fundamental positive-sequence component, which is transformed into dc quantities in the d and q axes, can be easily extracted by low-pass filters (LPFs). Also, all harmonic components are transformed into ac quantities with a fundamental frequency shift

$$i_{l,d} = \tilde{i}_{l,d} + \bar{i}_{l,d} \quad (3)$$

$$i_{l,q} = \tilde{i}_{l,q} + \bar{i}_{l,q} \quad (4)$$

Where, $i_{l,d}, i_{l,q}$ are d - q components of load current, $\bar{i}_{l,d}, \bar{i}_{l,q}$ are dc components, and $\tilde{i}_{l,d}, \tilde{i}_{l,q}$ are the ac components of $i_{l,d}$ and $i_{l,q}$.

If i_s is the feeder current and i_{pf} is the shunt CSC current and knowing $i_s = i_l - i_{pf}$, then d - q components of the shunt CSC reference current are defined as follows:

$$i_{pf,d}^{ref} = i_{l,d} \quad (5)$$

$$i_{pf,q}^{ref} = i_{l,q} \quad (6)$$

Consequently, the d - q components of the feeder current are

$$i_{s,d} = \tilde{i}_{l,d} \quad (7)$$

$$i_{s,q} = 0 \quad (8)$$

This means that there are no harmonics and reactive Components in the feeder current. Switching losses cause the dc-link capacitor voltage to decrease.

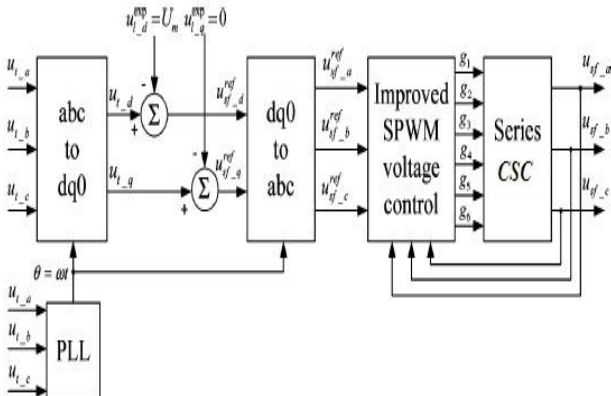


Fig.5. Control block diagram of the series CSC

Other disturbances, such as the sudden variation of the load, can also affect the dc link. In order to regulate the dc-link capacitor voltage, a proportional-integral (PI) controller is used as shown in Fig. 4. The input of the PI controller is the error between the actual capacitor voltage (u_{dc}) and its reference value (u_{dc}^{ref}). The output of the PI controller (i.e., Δi_{dc}) is added to the d component of the shunt-CSC reference current to form a new reference current as follows:

$$\begin{cases} i_{pf,d}^{ref} = \tilde{i}_{l,d} + \Delta i_{dc} \\ i_{pf,q}^{ref} = i_{l,q} \end{cases} \quad (9)$$

As shown in Fig. 4, the reference current in (9) is then transformed back into the abc reference frame. By using PWM hysteresis current control, the output-compensating currents in each phase are obtained

$$i_{pf-abc}^{ref} = T_{dq0}^{abc} i_{pf-dq0}^{ref}; (T_{dq0}^{abc} = T_{abc}^{dq0-1}) \quad (10)$$

Series-CSC: Functions of the series CSC's in each feeder are:

- 1) To mitigate voltage sag and swell;
- 2) To compensate for voltage distortion, such as harmonics;
- 3) To compensate for interruption (in Feeder2 only).

The control block diagram of each series CSC is shown in Fig. 5. The bus voltage ($u_{t,abc}$) is detected and then transformed into the synchronous $dq0$ reference and then transformed into the synchronous $dq0$ reference frame using

$$u_{t,dq0} = T_{abc}^{dq0} u_{t,abc} = u_{t1p} + u_{t1n} + u_{t10} + u_{th} \quad (11)$$

Where

$$\begin{cases} u_{t1p} = [u_{t1p,d} \ u_{t1p,q} \ 0]^T \\ u_{t1n} = [u_{t1n,d} \ u_{t1n,q} \ 0]^T \\ u_{t10} = [0 \ 0 \ u_{t10}]^T \\ u_{th} = [u_{th,d} \ u_{th,q} \ u_{th,0}]^T \end{cases} \quad (12)$$

u_{t1p} , u_{t1n} and u_{t10} are fundamental frequency positive, negative, and zero-sequence components, respectively, and u_{th} is the harmonic component of the bus voltage.

According to control objectives of the CSC-UPQC, the load voltage should be kept sinusoidal with constant amplitude even if the bus voltage is disturbed. Therefore, the expected load voltage in the synchronous $dq0$ reference frame ($u_{l,dq0}^{exp}$) only has one value

$$u_{l,dq0}^{exp} = T_{abc}^{dq0} u_{l,abc}^{exp} = \begin{bmatrix} u_m \\ 0 \\ 0 \end{bmatrix} \quad (13)$$

Where the load voltage in the abc reference frame ($u_{l,abc}^{exp}$) is

$$u_{l,abc}^{exp} = \begin{bmatrix} u_m \cos(\omega t) \\ u_m \cos(\omega t - 120^\circ) \\ u_m \cos(\omega t + 120^\circ) \end{bmatrix} \quad (14)$$

The compensating reference voltage in the synchronous $dq0$ reference frame ($u_{sf,dq0}^{ref}$) is defined as

$$u_{sf,dq0}^{ref} = u_{t,dq0} - u_{l,dq0}^{exp} \quad (15)$$

This means $u_{t1p,d}$ in (12) should be maintained at U_m while all other unwanted components must be eliminated. The compensating reference voltages in (15) are then transformed back into the abc reference frame.

By using an improved SPWM voltage control technique (since PWM control with minor loop feedback) [8], the output compensation voltage of the series CSC can be obtained.

D. Designing & Controller of Fuzzy logic Technique:

The word Fuzzy means vagueness. Fuzziness occurs when the boundary of piece of information is not clear-cut. In 1965 Lotfi A.Zahed propounded the fuzzy set theory. Fuzzy set theory exhibits immense potential for effective solving of the uncertainty in the problem. Fuzzy set theory is an excellent mathematical tool to handle the uncertainty arising due to vagueness. Understanding human speech and recognizing handwritten characters are some common instances where fuzziness manifests. Fuzzy set theory is an extension of classical set theory where elements have varying degrees of membership. Fuzzy logic uses the whole interval between 0 and 1 to describe human reasoning. In FLC the input variables are mapped by sets of membership functions and these are called as “FUZZY SETS”.

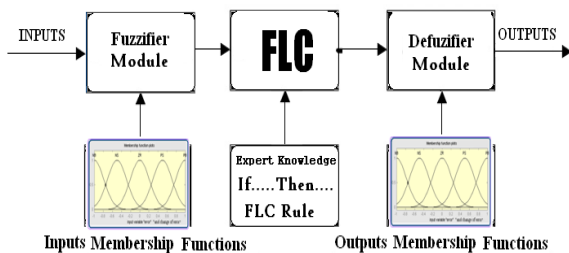


Fig.6. Fuzzy Basic Module Block Diagram

Fuzzy set comprises from a membership function which could be defined by parameters. The value between 0 and 1 reveals a degree of membership to the fuzzy set. The process of converting the crisp input to a fuzzy value is called as “Fuzzification.” The output of the Fuzzier module is interfaced with the rules. The basic operation of FLC is constructed from fuzzy control rules utilizing the values of fuzzy sets in general for the error and the change of error and control action.

The results are combined to give a crisp output controlling the output variable and this process is called as “DEFUZZIFICATION.” Fig.6 control strategy based on 49 Fuzzy controls Rule with combination of Seven error states multiplying with seven change of error states.

Table 1: Represents the Fuzzy Rules

e	Δe	NL	NM	NS	ZR	PS	PM	PL
NL		NL	NL	NL	NL	NL	NL	NL
NM		NL	NL	NM	NM	NS	NS	NS
NS		NL	NM	NM	NS	NS	NS	ZR
ZR		ZR	ZR	ZR	ZR	ZR	ZR	ZR
PS		ZR	PS	PS	PS	PM	PM	PL
PM		PS	PS	PS	PM	PM	PL	PL
PL		PL	PL	PL	PL	PL	PL	PL

III. POWER-RATING ANALYSIS OF CSC-UPQC

The power rating of the CSC-UPQC is an important factor in terms of cost. Before calculation of the power rating of each CSC in the CSC-UPQC structure, two models of a UPQC are analyzed and the best model which

requires the minimum power rating is considered. All voltage and current phasors used in this section are phase quantities at the fundamental frequency.

There are two models for a UPQC-quadrature compensate (UPQC-Q) and inphase compensation (UPQC-P). In the quadrature compensation scheme, the injected voltage by the series-CSC maintains a quadrature advance relationship with the supply current so that no real power is consumed by the series CSC at steady state. This is a significant advantage when UPQC mitigates sag condition. The series CSC also shares the Volt-Ampere Reactive (VAR) of the load with the shunt-CSC, reducing the power rating of the shunt-CSC.

Fig. 7 shows the phasor diagram of the scheme under a typical load power factor condition with and without voltage sag. When the bus voltage is at the desired value ($U_l = U_t = U_0$), the series-injected voltage (U_{sf}) is zero shown in Fig. 7(a). The shunt CSC injects the reactive component of the load current I_c , resulting in unity input-power factor. Furthermore, the shunt CSC compensates for not only the reactive component, but also the harmonic components of the load current. For sag compensation in this model, the quadrature series voltage injection is needed as shown in Fig. 7(b). The shunt CSC injects I_c in such a way that the active power requirement of the load is only drawn from the utility which results in a unity input-power factor.

In an inphase compensation scheme, the injected voltage is inphase with the supply voltage when the supply is balanced. By virtue of inphase injection, series CSC will mitigate the voltage sag condition by minimum injected voltage. The phasor diagram of Fig. 7 explains the operation of this scheme in case of voltage sag.

A comparison between inphase (UPQC-P) and quadrature (UPQC-Q) models is made for different sag conditions and load power factors in [13]. It is shown that the power rating of the shunt-CSC in the UPQC-Q model is lower than that of UPQC-P, and the power rating of the series-CSC in the UPQC-P model is lower than that of the UPQC-Q for a power factor of less than or equal to 0.9. Also, it is shown that the total power rating of UPQC-Q is lower than that of UPQC-P where the VAR demand of the load is high.

As discussed in Section II, the power needed for interruption compensation in Feeder2 must be supplied through the shunt CSC in Feeder1 and the series CSC in Feeder2. This implies that power ratings of these CSCs are greater than that of the series one in Feeder1. If quadrature compensation in Feeder1 and inphase compensation in Feeder2 are selected, then the power rating of the shunt CSC and the series CSC (in Feeder2) will be reduced. This is an important criterion for practical applications.

Based on the aforementioned discussion, the power-rating calculation for the CSC-UPQC is carried out on the basis of the linear load at the fundamental frequency. The parameters in Fig.7 are corrected by adding suffix “1,” indicating Feeder1, and the parameters in Fig. 8 are corrected by adding suffix “2,” indicating Feeder2. As shown in Fig. 7 and 8, load voltages in both feeders are kept constant at U_0 regardless of bus voltages variation,

and the load currents in both feeders are assumed to be constant at their rated values (i.e., I_{01} and I_{02} , respectively)

$$U_{l1} = U_{l2} = U_0 \quad (16)$$

$$\begin{cases} I_{l1} = I_{01} \\ I_{l2} = I_{02} \end{cases} \quad (17)$$

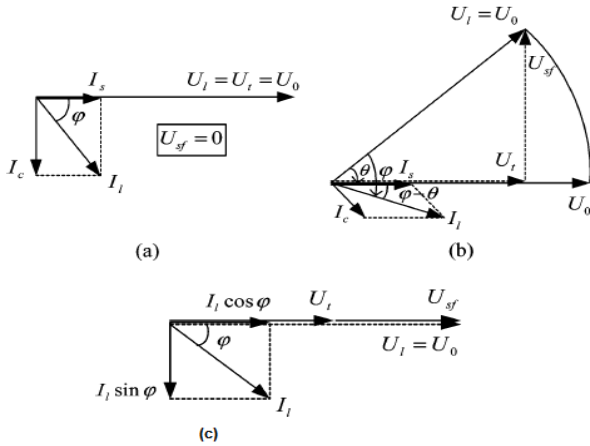


Fig.7. Quadrature Compensation Phasor diagrams.

- (a) Without voltage sag (b) with voltage sag
(c) Phasor diagram of in phase compensation (supply voltage sag)

The load power factors in Feeder1 and Feeder2 are assumed to be $\cos \phi_1$ and $\cos \phi_2$ and the per-unit sags, which must be compensated in Feeder1 and Feeder2, are supposed to be x_1 and x_2 , respectively.

If the CSC-UPQC is lossless, the active power demand supplied by Feeder1 consists of two parts:

- 1)The active power demand of load in Feeder1;
- 2)The active power demand for sag and interruption compensation in Feeder2. Thus, Feeder1 current (I_{s1}) can be found as

$$U_{t1} I_{s1} = U_{l1} I_{l1} \cos \phi_1 + U_{sf2} I_{l2} \cos \phi_2 \quad (18)$$

$$(1-x_1) I_{s1} = I_{01} \cos \phi_1 + x_2 I_{02} \cos \phi_2 \quad (19)$$

$$I_{s1} = \frac{I_{01} \cos \phi_1}{(1-x_1)} + \frac{x_2 I_{02} \cos \phi_2}{(1-x_1)} \quad (20)$$

From Fig. 6, the voltage injected by the series CSC in Feeder1 can be written as in (22) and, thus, the power rating of this converter (S_{VSC1}) can be calculated as

$$U_{sf1} = U_{t1} \tan \theta = U_0 (1-x_1) \tan \theta \quad (21)$$

$$S_{VSC1} = 3U_{sf1} I_{s1} = 3U_0 (1-x_1) \tan \theta \quad (22)$$

The shunt CSC current is divided into two parts.

- 1)The first part (i.e., I_{c1}) compensates for the reactive components and harmonic components of Feeder1 current and can be calculated from Fig. 7 as

$$\begin{aligned} I_{c1} &= \sqrt{I_{l1}^2 + I_{s1}^2 - 2I_{l1} I_{s1} \cos(\phi_1 - \theta)} \\ &= \sqrt{I_{01}^2 + I_{s1}^2 - 2I_{01} I_{s1} \cos(\phi_1 - \theta)} \end{aligned} \quad (23)$$

Where I_{s1} is calculated in (21). This part of the shunt CSC current only exchanges reactive power (Q) with the system.

- 2)The second part provides the real power (P), which is needed for sag or interruption compensation in Feeder2. Therefore, the power rating of the shunt CSC can be calculated as

$$\begin{aligned} S_{VSC2} &= 3U_{l1} I_{pf} = 3\sqrt{Q^2 + P^2} \\ &= 3U_0 \sqrt{I_{c1}^2 + (x_2 I_{02} \cos \phi_2)^2} \end{aligned} \quad (24)$$

Where I_{c1} is calculated in (24)

Finally, the power rating of the series-CSC in Feeder2 can be calculated by (25). For the worst-case scenario (i.e., interruption compensation), one must consider $x_2 = 1$. Therefore

$$S_{VSC3} = 3U_{sf2} I_{l2} = 3x_2 U_0 I_{02} \quad (25)$$

IV. SIMULATION RESULTS

The proposed CSC-UPQC and its ANN control schemes have been tested through extensive case study simulations using MATLAB/PSCAD. In this section, simulation results are presented, and the performance of the proposed CSC-UPQC system is shown.

A. Distortion and sag/swell on the Bus voltage

Let us consider that the power system in Fig. 2 consists of two three-phase three-wire 380(v) (RMS, L-L), 50-Hz utilities. The BUS1 voltage (u_{t1}) contains the seventh-order harmonic with a value of 22%, and the BUS2 voltage (u_{t2}) contains the fifth-order harmonic with a value of 35%. The BUS1 voltage contains 25% sag between $0.1 \text{ s} < t < 0.2 \text{ s}$ and 20% swell between $0.2 \text{ s} < t < 0.3 \text{ s}$. The BUS2 voltage contains 35% sag between $0.15 \text{ s} < t < 0.25 \text{ s}$ and 30% swell between $0.25 \text{ s} < t < 0.3 \text{ s}$. The nonlinear/sensitive load L1 is a three-phase rectifier load which supplies an RC load of 10Ω and $30 \mu\text{F}$. Finally, the critical load L2 contains a balance RL load of 10Ω and 100mH .

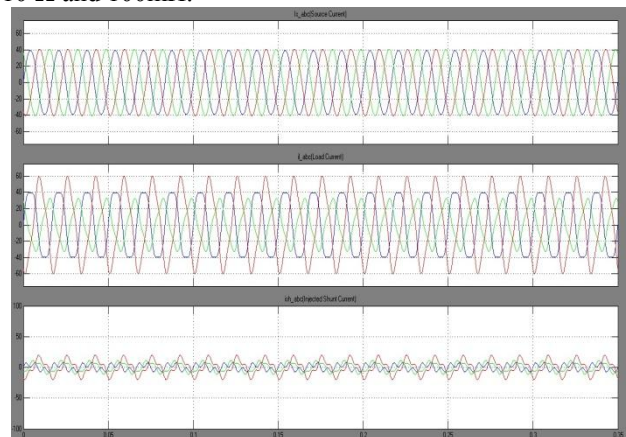


Fig.8. Voltage Harmonics at t=0.1sec to 0.2sec Compensation with Fuzzy Technique

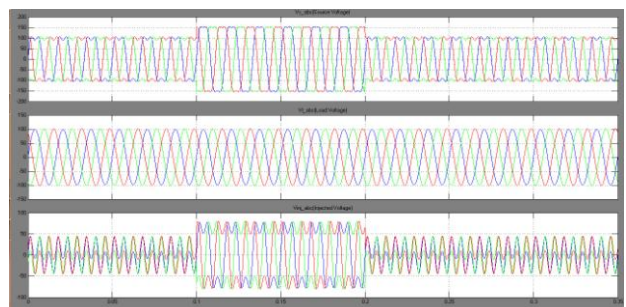


Fig.9. Voltage Swell at t=0.1sec to 0.2sec compensation with Fuzzy Technique

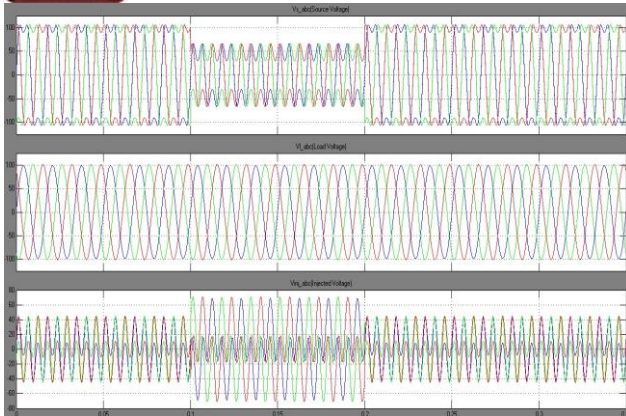


Fig.10. Voltage Sag at t=0.1sec to 0.2sec compensation with Fuzzy Technique

The CSC-UPQC is switched on at $t = 0.02$ s. The BUS1 voltage, the corresponding compensation voltage injected by CSC1 and finally load L1 voltage are shown in Fig. 8. In all figures, only the phase *a* waveform is shown for simplicity.

Similarly, the BUS2 voltage, the corresponding compensation voltage injected by CSC3, and finally, the load L2 voltage are shown in Fig. 9. As shown in these figures, distorted voltages of BUS1 and BUS2 are satisfactorily compensated for across the loads L1 and L2 with very good dynamic response.

The nonlinear load current, its corresponding compensation current injected by CSC2, compensated Feeder1 current, and, finally, the dc-link capacitor voltage are shown in Fig. 10. The distorted nonlinear load current is compensated very well, and the total harmonic distortion (THD) of the feeder current is reduced from 28.5% to less than 5%. Also, the dc voltage regulation loop has functioned properly under all the disturbances, such as sag/swell in both feeders. One of the many solutions is the use of a combined system of shunt and Series converter like multi converter unified power quality conditioner (CSC-UPQC). compensate the supply voltage and the load current or to mitigate any type of voltage and current fluctuations sag, swell and power factor correction in a power distribution network. The control strategies used here are based on PI & ANN controller of the CSC-UPQC in detail. The control strategies are modeled using MATLAB/SIMULINK. The simulation results are listed in comparison of different control strategies are shown in figures 9, 10, 11, 12 and 13.

V. CONCLUSION

The present topology illustrates the operation and control of Multi Converter Unified Power Quality Conditioner (CSC-UPQC). The power quality problems in distribution systems are not new but customer awareness of these problems increased recently. It is very difficult to maintain electric power quality at acceptable limits. One modern and very promising solution that deals with both load current and supply voltage imperfections is the Unified Power Quality Conditioner (CSC-UPQC). Proposed model for the CSC-UPQC is to

compensate input voltage harmonics and current harmonics caused by non-linear load. This paper presented review on the UPQC to enhance the electric power quality at distribution level. The CSC-UPQC is able to compensate supply voltage power quality issues such as, sags, swells, unbalance, flicker, harmonics, and for load current power quality problems such as, harmonics, unbalance, reactive current and neutral current With PID & Fuzzy Controller. In this paper several UPQC configurations have been discussed. Among all these configurations, UPQC - DG could be the most interesting topology for a renewable energy based power system.

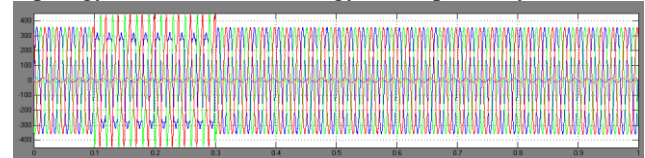


Fig.11. Three Phase Source Voltage (V_a, V_b, V_c) Waveform

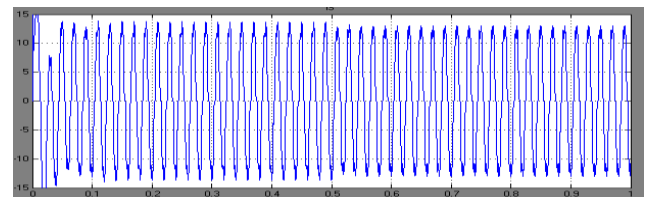


Fig.12. Load Current with Fuzzy Controller

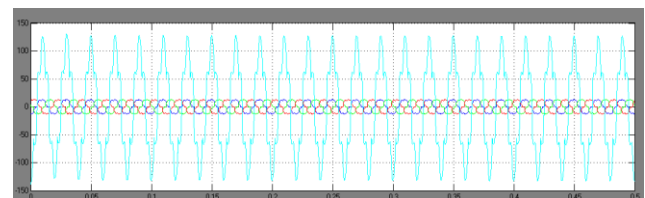


Fig.13. Load Voltage with Fuzzy Controller

REFERENCES

- [1] Hamid Reza Mohammadi, Ali Yazdian Varjani, and Hossein Mokhtari, "Multiconverter Unified Power-Quality Conditioning System: CSC-UPQC" IEEE RANSACTIONS ON POWER DELIVERY, VOL. 24, NO. 3, JULY 2009.
- [2] R.Rezaei pour and A.Kazemi, "Review of Novel control strategies for UPQC" Internal Journal of Electric and power Engineering 2(4) 241-247, 2008.
- [3] S. Ravi Kumar and S.Siva Nagaraju "Simulation of DSTATCOM and DVR in power systems" Vol. 2, No. 3, June 2007 ISSN 1819-6608 ARPN Journal of Engineering and Applied Sciences.
- [4] M.V.Kasuni Perera "Control of a Dynamic Voltage Restorer to compensate single phase voltage sags" Master of Science Thesis, Stockholm, Sweden 2007.
- [5] M. Basu, S. P. Das, and G. K. Dubey, "Comparative evaluation of two models of UPQC for suitable interface to enhance power quality," *Elect. Power Syst. Res.*, pp. 821-830, 2007.
- [6] A. K. Jindal, A. Ghosh, and A. Joshi, "Interline unified power quality conditioner," *IEEE Trans. Power Del.*, vol. 22, no. 1, pp. 364-372, Jan. 2007.
- [7] B. Singh, K. Al-Haddad, and A. Chandra, "A review of active power filters for power quality improvement," *IEEE Trans. Ind. Electron.*, vol. 45, no. 5, pp. 960-971, Oct. 1999.
- [8] C. A. Quinn and N.Mohan, "Active filtering of harmonic currents in three-phase, four-wire systems with three-phase and single-phase nonlinear loads," in *Proc. 7th IEEE APEC*, 1992, pp. 829-836.

- [9] H. Akagi, Y. Kanazawa, and A. Nabae, "Instantaneous reactive power compensators comprising switching devices without energy storage components," *IEEE Trans. Ind. Appl.*, vol. IA-20, no. 3, pp. 625-630, May/June 1984.
- [10] Y. Komatsu and T. Kawabata, "A control method of active power filter in unsymmetrical and distorted voltage system," in *Proc. Conf. IEEE Power Convers.*, 1997, vol. 1, pp. 161-168.
- [11] M. T. Haque, "Single-phase PQ theory," in *Proc. 33rd IEEE PESC*, 2002, vol. 4, pp. 1815-1820.
- [12] J. M. Correa, S. Chakraborty, M. G. Simoes, and F. A. Farret, "A singlephase high frequency AC microgrid with an unified power quality conditioner," in *Conf. Rec. 38th IEEE IAS Annu. Meeting*, 2003, vol. 2, pp. 956-962.
- [13] V. Khadkikar, A. Chandra, A. O. Barry, and T. D. Nguyen, "Application of UPQC to protect a sensitive load on a polluted distribution network," in *Proc. IEEE PES General Meeting*, Montreal, QC, Canada, 2006, 6 pp.
- [14] V. Khadkikar, A. Chandra, A. O. Barry, and T. D. Nguyen, "Conceptual analysis of unified power quality conditioner (UPQC)," in *Proc. IEEE ISIE*, 2006, pp. 1088-1093.
- [15] M. Aredes, K. Heumann, and E. H. Watanabe, "An universal active power line conditioner," *IEEE Trans. Power Del.*, vol. 13, no. 2, pp. 545-551, Apr. 1998.
- [16] R. Faranda and I. Valade, "UPQC compensation strategy and design aimed at reducing losses," in *Proc. IEEE ISIE*, 2002, vol. 4, pp. 1264-1270.

AUTHORS PROFILE



Ch. Suresh Kumar

was born in Kakinada, AP, India in 1974. He received DEEE from SBTET and he received his B.Tech degree from JNTU. The Author is pursuing M.Tech in Power Electronics and Electrical Drives from St. Theresa Institute of Technology and Management, Garividi, Vizianagaram Dist. AP.

India.

He has a hand full of rich experience in Erection, testing and commissioning, operation and maintenance of Plant Electrical Packages. At present, he is working as a Deputy Manager – Electrical in a Coal Based Thermal Power Plant which is under construction.



G. Shiva Ram Prasad

was born in Hyderabad, India, in 1985. He received the B.Tech degree from TRR College of Engg & Management and he received M.Tech (Power Electronics) degree from JNTU. He worked as an electrical engineer in Energy Infratech Pvt Ltd from 2010 to 2013. At present, he is working as Testing

Engineer in Kernex Microsystems India Ltd. His areas of interests include, Power Quality, Solar Power Generation, Railway Safety Equipment & Wireless Power Transmission.

B. Shankar Prasad

was born in Vizianagaram, India. He has been working as an Associate Professor and Head of the Electrical and Electronics Department in St. Theresa institute of management and Technology. He has more than 10 years of experience in teaching in almost all the core related subjects and given guidance many projects in graduate level as well as in postgraduate level. (Photo not available)