

Bluetooth Based Synthesizer for Wireless Sensor Measurements

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Abstract – In this paper aims to overcome the spur problems in Bluetooth-based wireless sensors measurement a compact fractional-N frequency synthesizer is presented ranging from 2 GHz to 3 GHz in frequency. Through this technique, the phase noise in the final spectrum is improved and spur tones in the output are deleted. Simple M-bit dither generator (Linear Feedback Shift Register) is deployed in an effective way to eliminate spur tones from fractional modulation. To validate the presented fractional-N frequency synthesizer with 26 MHz reference frequency, we utilize TSMC 0.18 um technology in ADS (Advanced Design System). The simulation results demonstrate that the used techniques make the fractional-N synthesizer's performance considerably better.

Keywords – Fractional-N, Noise Cancellation, LFSR, Spurs.

I. INTRODUCTION

Wireless sensors play an important role in many remote sensing and monitoring applications. Furthermore, Frequency synthesizers are the heart of each wireless transmitter/receiver system [1-4]. Almost every communications consumer product employs a frequency synthesizer often operated as a local oscillator providing the carrier frequency of interest. At its simplest, due to the fact that an Integer-N PLL is limited by integer multiples N of a fixed crystal frequency, it fails to achieve a wide tenability and a fine resolution [5]. Additionally, its phase noise performance is degraded owing to large values of N. Fractional-N PLLs [6], can solve this limitation by allowing for fractional multiplication of reference frequency by enabling the use of a high-frequency reference signal and much lower division values while it still maintains the required resolution [6]. In these frequency synthesizers, the output sequence of Sigma-Delta modulator changes the division ratio and as a result, it changes the frequency resolution. The $\Sigma\Delta$ offers two very desirable properties: noise shaping and randomization. It can shape quantization noise to higher frequency offsets, and reduce noise near the carrier frequency. . The synthesizer which uses higher reference frequencies has wider loop band-widths, causing in-band VCO phase noise to be reduced. Every block of synthesizer contributes in degrading the total phase noise figure. For elimination of the spur tones and to improve the phase noise specifications, high order $\Sigma\Delta$ modulators with enough quantization levels are usually used [7]. On the other hand, if the $\Sigma\Delta$ modulator's order is higher than the synthesizer's order, the phase noise is affected. To solve this problem, the complex $\Sigma\Delta$ modulator architecture was used resulting in increasing in the number

of hardware parts and cost [8].

In this paper, two techniques are used to reduce above-mentioned problems. First, a technique for reduction in spur tones magnitudes for MASH $\Sigma\Delta$ modulator is used. The contribution of this work relies on the use of close-form equations [9] to characterize the digital $\Sigma\Delta$ modulator periodicity when a dither signal from a LFSR is added as a least significant bit (LSB). Equations show that a very simple dither generator (LFSR) can make the periodicity disabled, if it is added to effective paths [9]. The rest of the paper is organized as following: in section II, general description of frequency synthesizer and MASH architecture is presented. In section III, we employ Proposed Fractional-N frequency synthesizer on making spur tone inactive to demonstrate that a very simple dither generator is effective to decrease the spur tone magnitude. In section IV, simulation results are considered and finally in section V, we conclude our findings.

II. GENERAL DESCRIPTION OF SYNTHESIZER AND MASH ARCHITECTURES

A. Fractional-N frequency synthesizer overview

Fig.1 shows a typical Fractional-N synthesizer. The goal of a fractional-N Synthesizer is to generate a periodic output signal with frequency $f_{out} = (N+\alpha)f_{ref}$, where N is an integer, α is a fractional value between 0 and 1 and f_{ref} is reference frequency of oscillator. As seen in this figure, a typical fractional-N synthesizer consists of such elements as a phase-frequency detector (PFD), a charge pump (CP), a loop filter, a voltage controlled oscillator (VCO), a frequency divider and a $\Sigma\Delta$ modulator [9]. The $\Sigma\Delta$ is utilized to generate a random sequence with a desired duty cycle to control the divider in the feedback path, and then an instantaneous phase error appears in the PFD input. The CP converts this phase error into current pulses and delivers charge to the loop filter. The loop filter voltage controls the VCO frequency and ensures that the fractional-N frequency remains locked. [10].

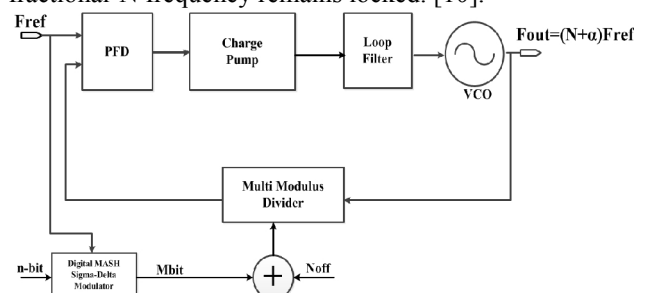


Fig.1. Typical Fractional-N Synthesizer

B. MASH architectures

The third order multi-stage noise shaping (MASH) [11] modulator is one of the most popular architectures, which is widely used in frequency synthesis. The MASH1-1-1 $\Sigma\Delta$ modulator is cascaded by three first order $\Sigma\Delta$ modulators. There are advantages that promote this architecture to become the focus of attention: its architectures with less complexity compared to the other entire third order $\Sigma\Delta$ modulators. To implement such a digital modulator, only three accumulators and latches are necessary. The over flow from each accumulator is 1-bit, so the noise cancellation logic is simple, which is similar to the pipelining technique. Also, the quantized output of each stage is processed by noise cancellation logic, as shown in Fig.2. The MASH modulators are unconditionally stable for any order, and the dynamic range consist of all the input quantization levels. The other significant merit of the MASH architecture is that it can work on much higher frequencies. Signal delays are cancelled by the following stage which can maximize sampling frequencies. Moreover, the noise transfer function has the same high-frequency behavior as some multi- loop architectures. Thus, the only disadvantage is high probability for this architecture to generate spur tones because of periodic behavior in the output [9].

To solve the problem several techniques are applied. These solutions are classified into two types –deterministic [11] and stochastic [12]. Deterministic approaches modify the digital $\Sigma\Delta$ modulator’s structure or set up an irrational condition to disrupt the modulator’s internal states. The advantages of this type of solutions are their controllable sequence length, or period, and furthermore, no low-frequency noise floor is incurred. Nowadays they are mainly used for MASH. On the other hand, the stochastic solution, also called dithering, is used for modulators. It uses a 1-bit pseudorandom (PN) sequence to scramble the Digital $\Sigma\Delta$ modulator’s input. Since dithering introduces an elevated noise floor at low frequencies, shaped dithering has been proposed to transfer the additive noise into a high-pass characteristic [12].

An unwanted task to implement the dithering is that the phase-noise generator has to be specifically designed with extra circuits. It is commonly realized with linear feedback shift registers (LFSR) [11], while another method employs another accumulator together with an 11-stage LFSR to dither the Digital $\Sigma\Delta$ modulator’s coefficients [12].

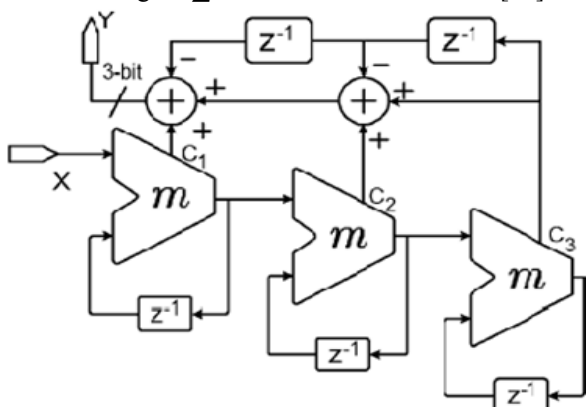


Fig .2: Digital Mash $\Sigma\Delta$ modulator

III. PROPOSED FRACTIONAL-N FREQUENCY SYNTHESIZER

Due to before section, in this section, a techniques applied to make the periodicity of the $\Sigma\Delta$ modulator’s output disabled.

First, based on [9] for an nth order digital MASH modulator the output signal is:

$$Y(z) = X(z) + (1 - z^{-1})^n E(z) \quad (1)$$

Where n is the modulator order and $E_n(z)$ is the quantization error of the last stage. In the digital MASH $\Sigma\Delta$ modulator, the quantization errors are deterministic and all of them are cancelled but the first in the last stage. This property makes the periodicity of quantization errors dependent on the input signal X and the quantization level $M=2^m$ (where m is the number of bits in the modulator) [10]. One of the most commonly used methods to break the periodicity of a digital $\Sigma\Delta$ modulator is to add a pseudo random signal as a least significant bit in the MASH modulators[9]. For those previous solutions it was proposed to add the dither signal at the input signal or within the MASH middle stages. In general, a very large LFSR was used but this increases the hardware complexity. In this research, the best way to add a pseudorandom sequence in a MASH 1-1-1 is shown in Fig.3 [9].

This can be achieved by only substituting the LSB in the input of the last two stages by the signal coming from an M-bit LFSR. This will not add more hardware to the modulator. The quantization errors for this case are [9]:

$$e_2(k) = \left[\frac{k(k+1)}{2} X + \frac{1}{M} \sum_{j=1}^k d(j) + e_1(0) + e_2(0) \right] \text{mod } M \quad (2)$$

and

$$e_2(n) = \left[\frac{n(n+1)(n+2)}{2} X + \frac{1}{M} \sum_{k=1}^n \sum_{j=1}^k d(j) + \sum_{k=1}^n d(k) + e_1(0) + e_2(0) + e_3(0) \right] \text{mod } M \quad (3)$$

For the quantization error to be periodic, i.e. $e_3[n] = e_3[n+N]$ and we can write [9]:

$$e_2(n) = \left[\frac{n(n+1)(n+2)}{2} X + \frac{1}{M} \sum_{k=1}^n \sum_{j=1}^k d(j) + \sum_{k=1}^n d(k) \right] \text{mod } M = 0 \quad (4)$$

Now, the double summation cannot be approximated to entire number that is divisible by M, because for every k value, the $d[j]$ values will not be uniformly distributed. With this way of adding the dither signal, the quantization error period N does not depend on the input value X. Whenever the dither signal is added as it is proposed in [9], the 3-bit output after the noise cancellation logic can be written as [9]:

$$Y(z) = X(z) + \frac{1}{M} D(z) \left((1 - z^{-1}) + (1 - z^{-1})^2 \right) + (1 - z^{-1})^2 E_3(z) \quad (5)$$

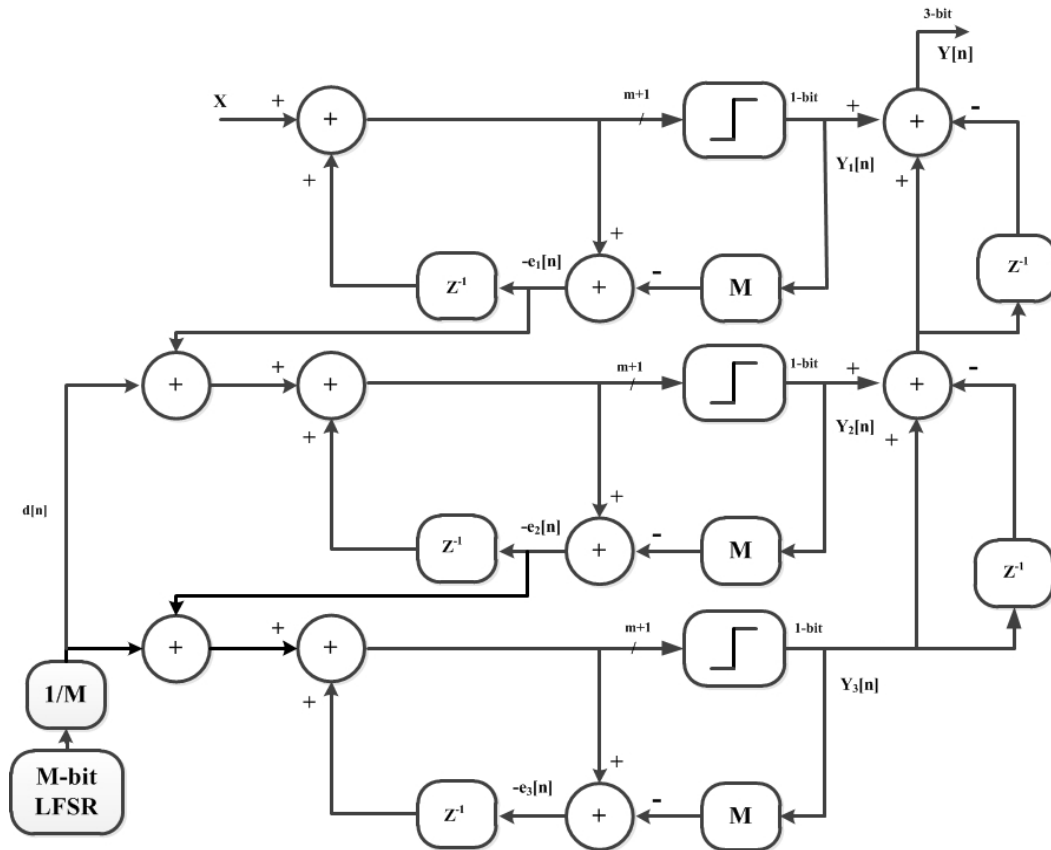


Fig. 3: applied solution to disable the periodicity in a MASH1-1-1 architecture

IV. SIMULATION RESULTS

We achieve simulation results of fractional-N PLL based on the proposed method by using 0.18um standard of CMOS in ADS. The model is the design of fully integrated multiband (0.9-3.6GHz) $\Sigma\Delta$ -Fractional-N PLL frequency synthesizer as well as for Bluetooth band of interest. It takes the advantages of a $\Sigma\Delta$ modulator to get a very fine frequency resolution and relatively large loop bandwidth. This frequency synthesizer is a fourth order charge pump PLL with 26MHz reference frequency. The loop bandwidth is about 150 KHz. Fig. 4 demonstrates the completed block diagram of the proposed fractional-N synthesizer.

The reference frequency is chosen 26 MHz. To create output frequency by the use of multi-modulus divider, the division ratio should be $(2.041101\text{GHz}/26\text{MHz})=78.5039$, and to realize the division ratio, the multi-modulus divider should cover all the moduli range from 75 to 85, so 6 asynchronous $\div 2/3$ dividers are required to build this multi-modulus. The MASH 1-1-1 has an 8-bit resolution in each accumulator, and the dither generator is a simple 8-bit LFSR. To save power and area, pipelining technique for $\Sigma\Delta$ modulator design and the modulator input number in binary is 01000001. The output of this LFSR according to Section III is applied to MASH modulator.

VCOs are widely used in frequency synthesizers to provide a local clock signal that can be locked to the frequency and phase of a reference signal. In this work, we utilize a Current-Starved VCO (CSVCO) topology

because of its wide frequency range of operation, allowing for tunable design that can easily accommodate the high-speed specifications in an RF application. A CSVCO is shown in Fig. 5 [13]. Its operation is similar to the ring oscillator. MOSFETs M2 and M3 operate as inverters while MOSFETs M1 and M4 operate as current sources which limit the available current of the inverter; in other words, the inverter is starved of current. MOSFETs M5 and M6 are mirrored/symmetric/the same in each inverter current source stage. The oscillation is achieved by charging and discharging the equivalent output capacitance in each stage of the VCO. This VCO is designed in TSMC 0.18 μm CMOS with operating frequency from 1.8GHz to 2.4 GHz. The simulated VCO phase noise is shown in Fig.6. We can see the phase noise is $-120\text{dBc}/\text{Hz}$ at 1MHz offset frequency.

V. CONCLUSION

This paper convinces us that spurious tones in the output of a fractional-N synthesizer can be eliminated by replacing the simple dither generator (8-bit LFSR) in an effective way. By using these simple methods, the number of elements is reduced and the circuit is compact rather than complicated methods.

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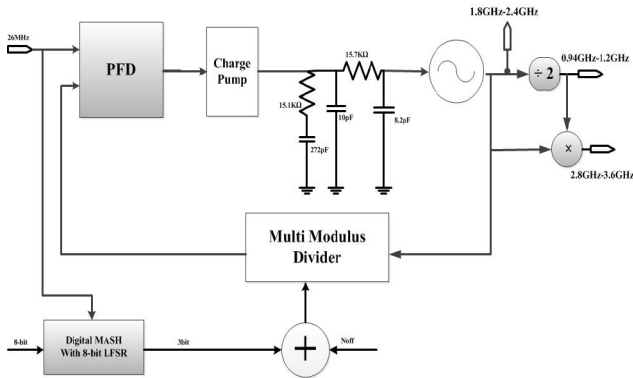


Fig.4. Complete block diagram of proposed fractional-N synthesizer

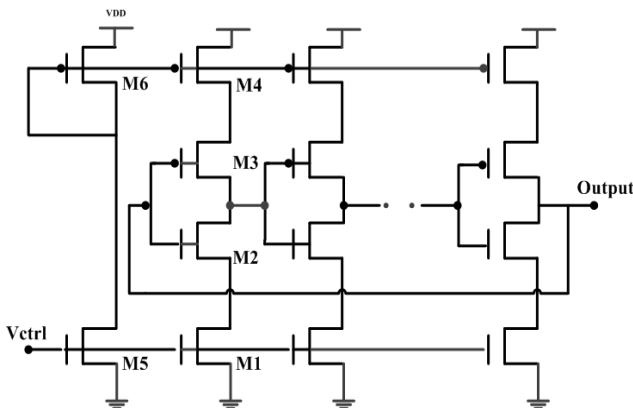


Fig.5. Circuit diagram of Current starved VCO

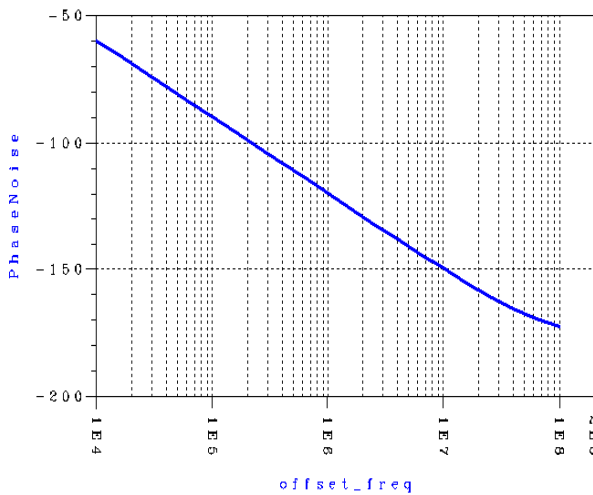


Fig.6. Simulated VCO block phase noise in Circuit result

Table I: Phase noise of the different bands

Frequency range	Phase noise @ 1MHz
0.94-1.2 GHz	-118dBc/Hz
1.8-2.4 GHz (Bluetooth band)	-115dBc/Hz
2.8-3.6 GHz	-106dBc/Hz

Table II: Specification of the Design

Technology	TSMC 0.18um CMOS
Supply	1.8V
Synthesizer Order	4

Reference Frequency	26 MHz
Frequency Range	0.94GHz – 3.6GHz
Frequency Bands	3
Loop Bandwidth	150 KHz
$\Sigma\Delta$ Architecture	3-bit MASH1-1-1

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