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Discrete Time Sigma-Delta Modulator with the Objective of Power Consumption Reduction with 130 um Technology

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Abstract **– In this paper a mono-loop discrete time sigma-delta modulator of order 2 is designed and implemented. The major aim of the design is to decrease the power consumption. To attain this goal this paper attempts to optimize the high power characteristic of the OTA modulators. Using an appropriate design and taking the power of biasing sources into account, the amplifier expends 1 mw for operation. At first, this modulator is simulated using MATLAB software as a system which encounters various conditions. The blocks of this modulator, in circuit level, are simulated with ADS software. The operational frequency of this modulator is 12 KHz whose ultra sampling rate is 256 for SNR>85dB.**

Keywords **– Sigma-Delta Modulator, OTA Modulators, ADS Software.**

I. INTRODUCTION

Sigma-delta modulator is a conventional method on which comprehensive examinations are made to convert an analogue signal to very high frequency digital series (J. C. Candy and G. C. Temes, 1992), (S. R. Northworthy, et. al., 1997). Among the major characteristics of sigma-delta modulatorsare: 1. A sampling rate more than nyquist rate, 2. Can use low resolution quantizers. 3. Energy of the noise in quantizer range of performance is removed from. Moreover, the sigma-delta modulators have the least sensitivity to the non-ideal characteristics of analogue elements. Therefore, it is the best option for high resolution applications like digital voice. Up to now, many delta-sigma-based modulators have been designed. However, most of these methods use 0.35 um technology with the power source amplitude of more than 3 volt. In this study the 0.13um technology with voltage source of 1.2v is used for the purpose of a low power circuit in conjunction with the low-power low-voltage digital auxiliary apparatus. To achieve this goal, and streamline the complexity of the design and also to warrant the stability, the modulator's structure is selected in form of a 2-order mono-loop structure in which the capacitor switching technique is utilized. The structure provides the discrete time calculation, low complexity and low power consumption. In first section, the simulation of different system conditions and feedback coefficient is performed via MATLAB software. Modulator design and simulation results are brought in next section. At the end, the total power consumption of the sigma-delta modulator of order 2 will be calculated. The ADS software is used for simulations.

II. DESIGN IN SYSTEM LEVEL

- *Modulator's structure*

Fig. 1 depicts a mono-polar sigma-delta Ideal modulator is calculated by Eq. 1. The OSR is ultra sampling rate and b indicates what bit-number the equalizer is. In this study b takes 1.

$$SNR_{peak} = \frac{3\pi}{2}(2^b - 1)(2n+1)(\frac{OSR}{\pi})^{2n+1} \qquad (1)$$

The primary issue of a multi bit sigma-delta is the linearity of equalizer. Therefore, in system part, the modulator is simulated for multi bit states. For the purpose of a better comparison, From Eq.1 for a 16-bit resolution the OSR (which OSR =fs/2fin) should be taken 256. It should be noted that for implementation of decimation filter, the OSR should be dyadic. By considering OSR=256 for a 1-bit modulator, the SNR is 19 dB. On this basis, the maximum SNR approximately yields a 17-bit resolution.

III. DESIGN IN CIRCUIT LEVEL

Fig.7 shows a differential tilted op-amp. The differential structures can achieve the gain, bandwidth as well as swing amplitude more than a mono-output amplifier could achieve. The use of PMOS inputs can remove the presence of chopper stabilization for less flicker noise than the NMOS type transistors (Mohammad Yavari and Omid Shoaei). One of the primary issues of nanometer technologies like 13nm technology is the small output impedance of the transistors. Therefore, applying them for higher gains is one of the major limitations of this technology. Taking the biasing sources into account, the provided gain-curve shows a gain about 52 dB and the CMRR= 63 dB as well as power consumption=1watt. In order to warrant the common mode voltage in fully differential amplifier, a CMFB circuit is considered in terms of a capacitor switch analogue to digital converter.

$$Ntf(z) = \frac{(1-z^{-1})^2}{1+z^{-1}(a_3a_4 + a_2a_3a_5 - 2) + z^{-2}(1-a_3a_4)} \qquad (3)$$

The second major element of this modulator is comparator or in other words 1-bit analogue to digital convertor. Since in this modulator, the 2-order noise shipping occurs, the modulator is not sensitive to principal defects of the comparator such as off-set hysteresis concerns etc. because this characteristic makes a

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relatively great noise (like Quintet noise) attenuated, this drawback could be attenuated as well. Totally, the critical challenge of the modulator design in circuit level relates to the first block. To realize this comparator, a structure called open surviving latch is used (see fig. 12)

Transistors M2,3 and M8,9 which are coupled in diagonal topology, are triggered by signal inserted to the drain instead of the source. In this way the block gating effect could be removed and the surviving rate could be promoted.

Watch generator circuit

A capacitor switch integrator needs 4 clocks (pulses) to operate appropriately; two signals have delayed to one another and the rest two signals are in non-overlapped form. Figure 19 shows the generation of these 4 signals. The delayed pulses are used to decrease the load discharge related to the input signal when the transistors are off.

Modulator circuit schematic

The 2-order modulator is appropriate for a 16-bit resolution. However, in high resolution modulators, the sampling capacitor value is determined by KT/C; the switching related noise. For fully differential modulator, by considering the switching noise, the SNR is:

$$SNR_{KT/C} = \frac{(2\times OL\times V_{ref})^2}{2}\times\frac{C_S\times OSR}{4KT} \qquad (2)$$

Holding C3= 1pf, the SNR calculated by E.q 2 is 106 dB. This value meets the 16-bit resolution. The following diagrams indicates the simulation results.

2-order sigma-delta modulator with coefficients a1 to a5 is:

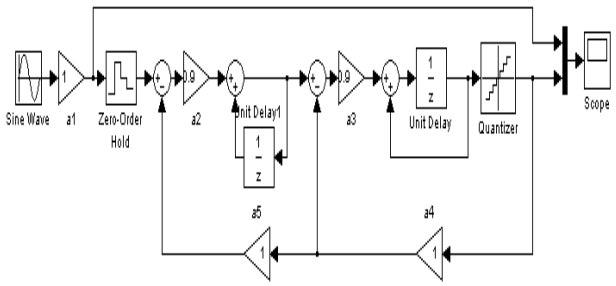

Fig.1. 1-bit modulator

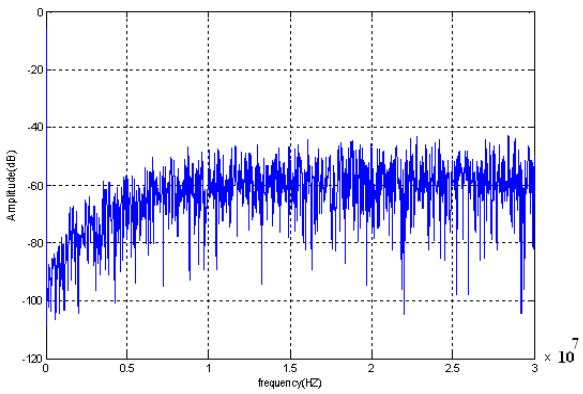

Fig.2. Order delta-sigma modulator

The system simulation results for different values of modulator coefficient are shown in table1. From table 1, the best case of the modulator parameters occurs when a1=0.8 and a2=0.8 while the rests take 1. The SNR value of this case is 102.6 dB. As regards 2-bit modulators, the values increase by 2-3dB. The increment calculated by Eg. 1 takes 3.7 dB.

Fig.2 presents the SNR diagram for 3 different input values. As shown, the SNR value gets the maximum value for a2=a3=0.8. Out of the 3 cases, the efficient bit value or ENOB can be calculated by:

$$ENOB = \frac{SNR - 1.76}{6.02} \qquad (5)$$

$$ENOB = 16.75 \quad @ \quad (a_2 = a_3 = 0.8)$$

$$ENOB = 16.3 \quad @ \quad (a_2 = a_3 = 0.7)$$

$$ENOB = 16.15 \quad @ \quad (a_2 = a_3 = 1)$$

Fig. 16 depicts the schematic of the 2-order mono-loop discrete time modulator. The modulator is controlled by a clock generator. To decrease the changes in samples and the short circuit resistance of the switches and to increase the linearity of the switches, all switches supposed to be CMOS type. One of the advantages of the capacitor-switch ADC circuits is that they don't need the S&H circuits. The S&H circuits pose a critical challenge in ADC design either for their high power consumption or for their complex designs. Invoking the presence of S&H circuits the complexity gets decreased and the major reduction in power consumption is yielded.

Power consumption calculation

In order to calculate the total power consumption of the modulator, power of each block is calculated and eventually all powers are aggregated. However, with the exclusion of op-amp circuits, all blocks consume dynamic power and with no clock the power consumption would be little and negligible.

$$OSR = 256,\ f_{in} = 10\ kHz,\ f_{sw} = 5.12\ MHz,\ V_{dd} = 1.2V,\ C_L \approx 1\ pf$$

$$p_{OTA} = I_d . V_{dd}$$

$$p_{dynamic} = \alpha_{\to 0} . C_L . V_{dd}{}^2 . f_{sw}$$

$$P_{total} = (2\times P_{OTA}) + (32\times P_{switch}) + (1\times P_{comparator}) + (2\times P_{DAC}) \approx 2.5\ mW$$

IV. Conclusion (I)

In this work a 2-order mono-loop delta-sigma modulator is simulated in discrete time domain. This method yields the SNR=95dB. The modulator blocks are also simulated in circuit level considering 0.13um technology. It was shown that the total power = 2.5w.

Table 1: The simulation results for 1-bit modulator

a_1	a_2	a_3	a_4	a_5	SNR(dB)	SFDR(dB)	DR(dB)
1	0.7	0.7	1	1	100	99.2	101
1	0.8	0.8	1	1	102.6	102	104
1	0.9	0.9	1	1	101.9	100.5	104.1
1	1	1	1	1	99	99	102
1	0.8	0.8	0.8	1	101.5	99.7	100.2
1	0.8	0.6	1	1	102.4	100	103
1	0.8	0.6	0.8	1	103	99.8	101.4
0.9	0.8	0.8	0.8	1	98.2	98	102

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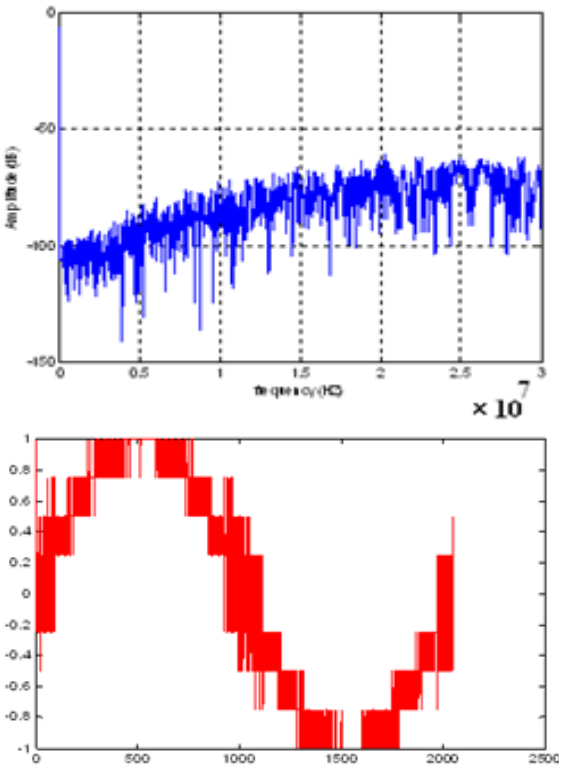

Fig.3. and Fig.4. 2-bit modulator' PSD output of 2-bit modulator

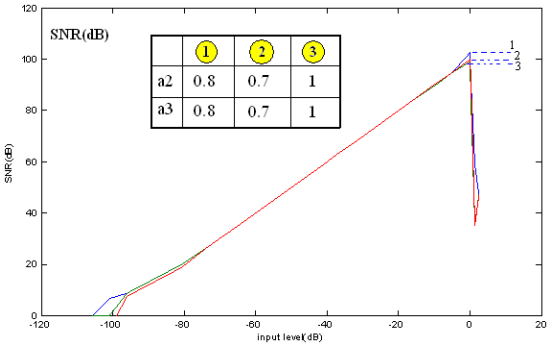

Fig.5. SNR Value

Power consumption calculation

In order to calculate the total power consumption of the modulator, power of each block is calculated and eventually all powers are aggregated. However, with the exclusion of op-amp circuits, all blocks consume dynamic power and with no clock the power consumption would be little and negligible.

$OSR = 256$, $f_{in} = 10\,kHz$, $f_{sw} = 5.12MHz$, $V_{dd} = 1.2V$, $C_L \approx 1pf$

$$p_{OTA} = I_d.V_{dd}$$

$$p_{dynamic} = \alpha_{\to 0}.C_L.V_{dd}^{\ 2}.f_{sw}$$

$$P_{total} = (2 \times P_{OTA}) + (32 \times P_{switch}) + (1 \times P_{comparator}) + (2 \times P_{DAC}) \approx 2.5mW$$

V. Conclusion (II)

In this work a 2-order mono-loop delta-sigma modulator is simulated in discrete time domain. This method yields the SNR=95dB. The modulator blocks are also simulated in circuit level considering 0.13um technology. It was shown that the total power = 2.5w.

Circuits' figure_ diagrams and tables simulated by ADS

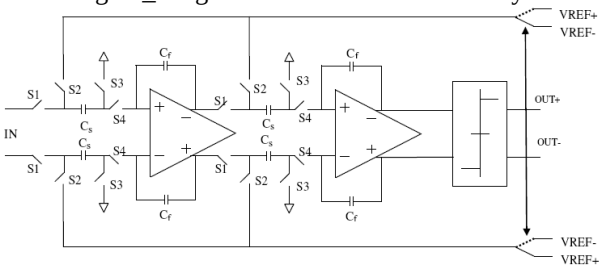

Fig.6 . The 2-order mono-loop discrete time modulator

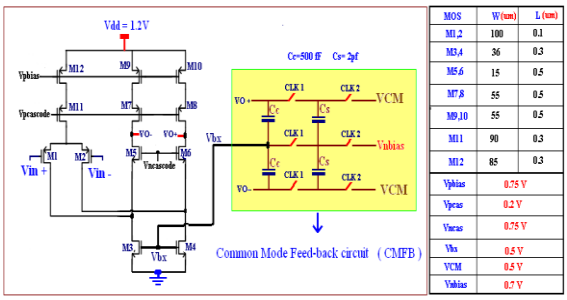

Fig. 7. Folded cascade OTA

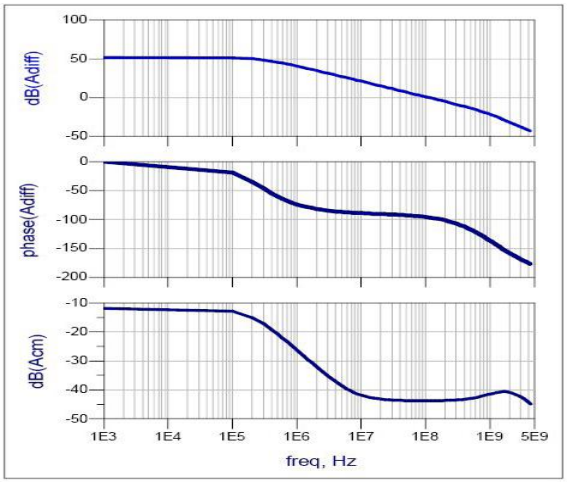

Fig.8. Op-amp frequency response.

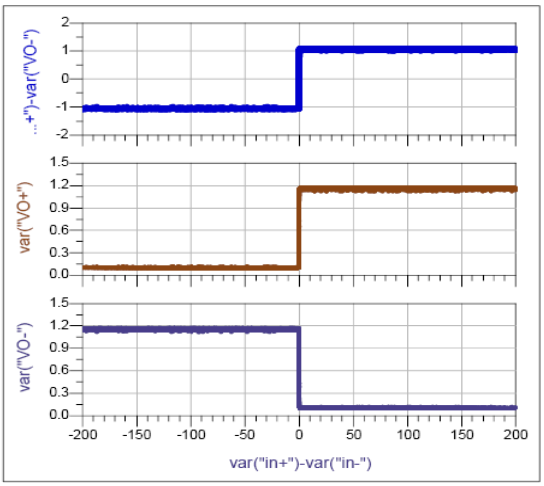

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Fig.9. Off-set voltage of op-amp (micro volt) Vos=10uv

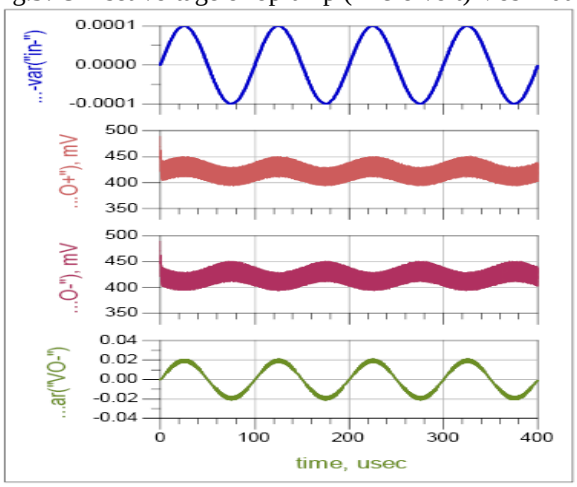


Fig.10. The output curve of op-amp in time domain and the CMFB effect in output voltage

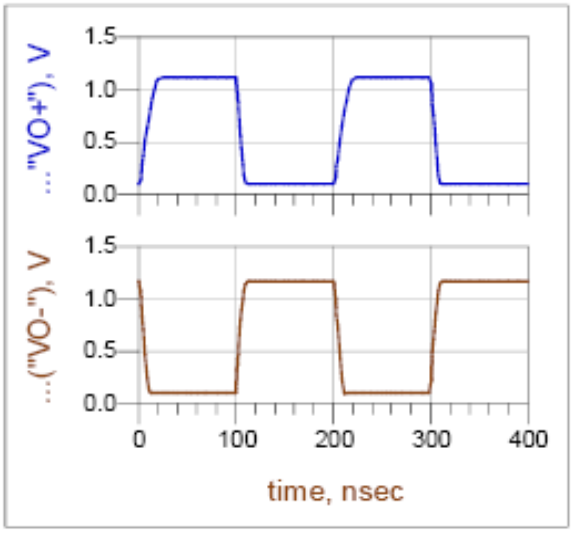
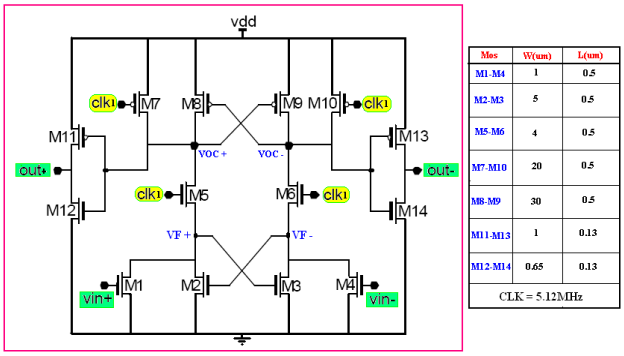


Fig. 11. SR curve

Figures associated with the comparator



Mos	W(um)	L(um)
M1-M4	1	0.5
M2-M3	5	0.5
M5-M6	4	0.5
M7-M10	20	0.5
M8-M9	30	0.5
M11-M13	1	0.13
M12-M14	0.65	0.13
CLK = 5.12MHz		

Fig.12. 1-bit comparator circuit

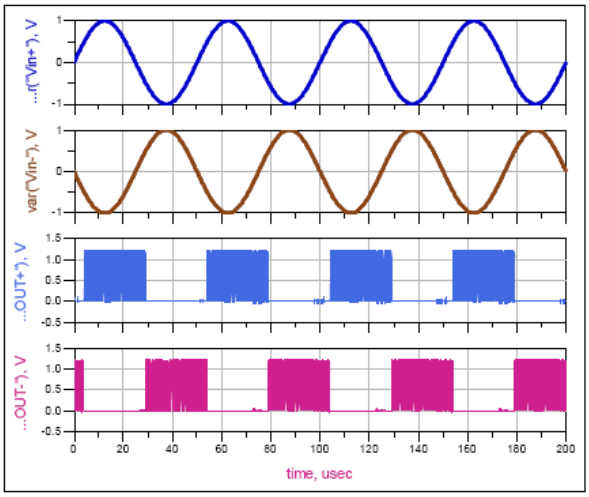


Fig.13. The time domain output for 2 sinusoidal inputs

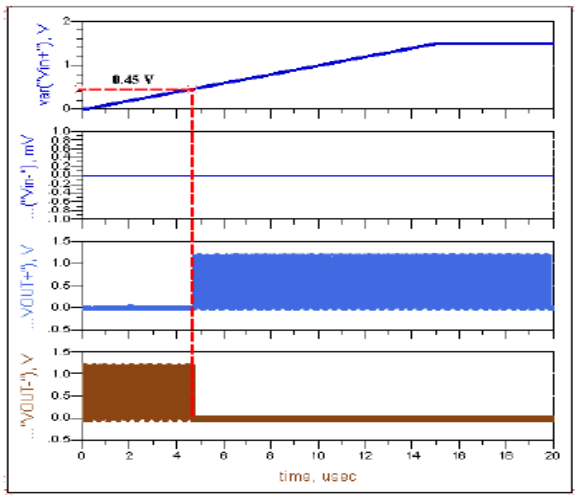
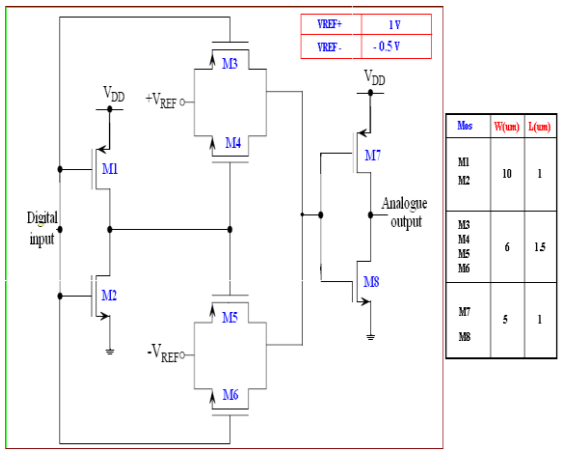


Fig.14. The minimum voltage difference between two inputs for toggling the output Vdiff(min)=0.45V

Figures associated with the 1-bit ADC



Mos	W(um)	L(um)
M1 M2	10	1
M3 M4 M5 M6	6	1.5
M7 M8	5	1

Fig.15. 1-bit ADC

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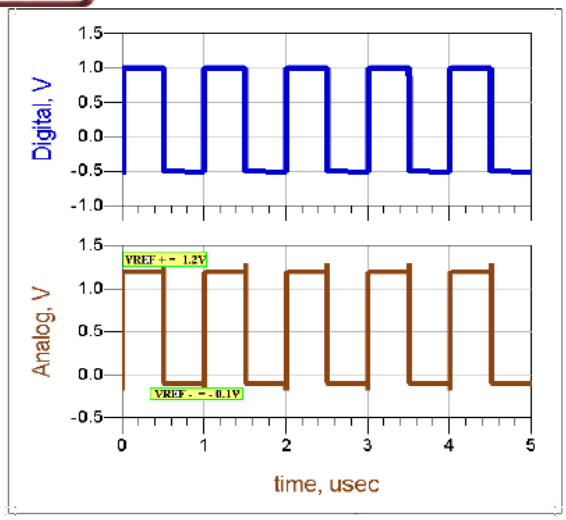

Fig.16. Input and output

Figures associated with the capacitor switch based integrator

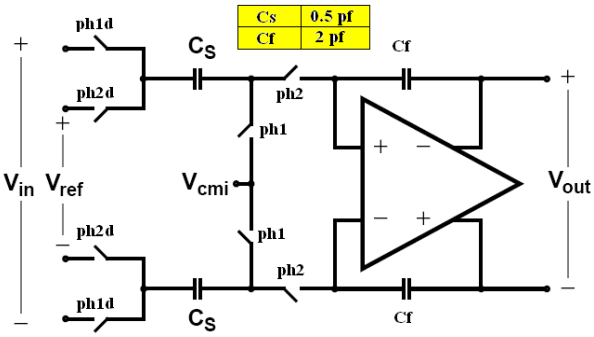

Fig.17. Capacitor switch- based integrator

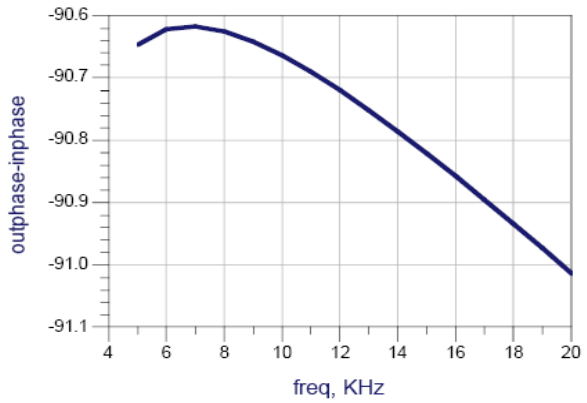

Fig.18. Integrator-made difference phase for sinusoidal input. 253 This difference is about 90 deg. For the frequency=10KHz

Figures associated with the clock generator

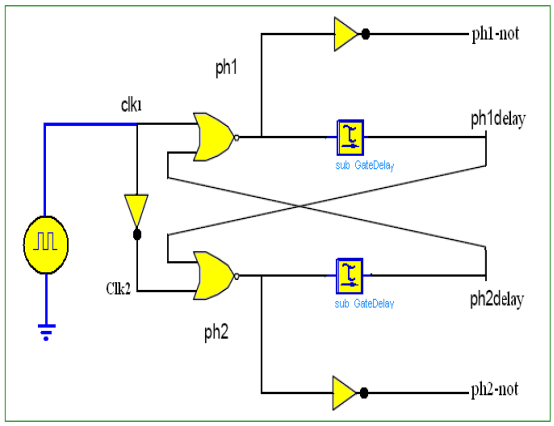

Fig.19. clock generator circuit

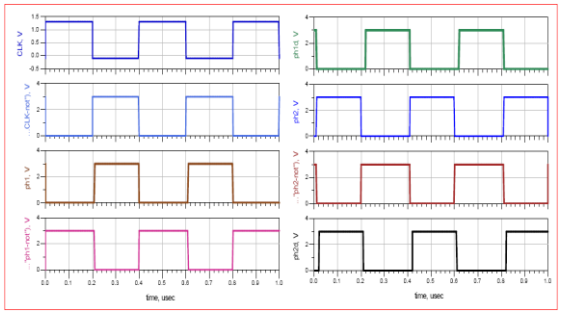

Fig.20. The curves generated by clock generator circuit(T-delay 10 nsec)

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