International Journal of Electronics Communication and Computer Engineering
Volume 5, Issue 4, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

Design of a CNFET-Based Programmable Frequency Divider with Division Ratio 2/3

Afshin KADIVARIAN
Department of Electrical Engineering
Science and Research Branch,
Islamic Azad University, Tehran, Iran
Email: afshin_kadivaryan@yahoo.com

Pooya TORKZADEH
Department of Electrical Engineering
Science and Research Branch,
Islamic Azad University, Tehran, Iran
Email: torkzadeh_oloom@yahoo.com

Gholamreza KARIMI
Department of Electrical Engineering
Faculty of Engineering
Razi University, Kermanshah, Iran
Email: ghkarimi@razi.ac.ir

***Abstract* – This paper describes a Carbon Nanotube Field Effect Transistor (CNFET)-based programmable frequency divider with division ratios 2 or 3. The proposed programmable frequency divider is composed of 3 Double Edge Flip-Flops and a 2:1 multiplexer. The important advantage of the proposed design is different division ratios that programmable with a switch and selector inputs of the multiplexer. This structure also has about 50% duty-cycle at the output signal. HSPICE based on CNFET model used to produce simulation results at 0.9 V supply voltage. Maximum power consumption of this work is 0. 07mW. Compared to other frequency dividers, simulations results show superior performance of the proposed design.**

***Keywords* – Programmable Frequency Divider, Carbon Nanotube Field Effect Transistor (CNFET), Double Edge Flip-Flop, Multiplexer.**

I. INTRODUCTION

A programmable frequency divider which divided an input frequency through programmable ratios is getting more consideration in RF-integrated circuits. Programmable dividers are largely applied to multiple clock signals on the same system-on-a-chip (SOC). In addition to produce variable clocksignals forswitched capacitor filters (SCFs). A programmable divider which can divide an input frequency by an ideal programmable ratio, making block of a frequency divider which used in a number of applications, such as frequency synthesis in clock generation, data recovery, mobile and satellite communication systems, synchronization and multiple-Gb/s opticfiber systems. Applying divisor numbers apart from 2^n for a quadrature LO generation, decreases the necessary frequency range of the synthesizer VCO. Low powerconsumption, wide division-ratio ranges,50% duty-cycle at the outputare the some of the common desired characteristics of the effective programmable frequency divider Ease of Use MOSFET technology came under more consideration. To outline noticeable characteristics of CNFET are lower power consumption comparedto MOSFET, higher efficiently and P-CNFET and N-CNFET, which having the same device geometries and mobilities and subsequently, the same current drive abilities, essential for transistorizing in the complex circuits [1-3].

Scaling down the size of CMOS technology in nanoranges can result in the following problems: short-channel effects (SCEs), high-power densities and reduced gate control and high sensitivity to method modifications. Due to the mention reason, scientists have done studies in nanotechnologies such as Single Electron Transistor (SET), Quantum-dot Cellular Automata (QCA), and Carbon Nanotube Field Effect Transistor (CNFET). Among them Carbon Nanotube Field Effect Transistor (CNFET) be caused of their most similarities with MOSFET technology came under more consideration. To outline noticeable characteristics of CNFET are lower power consumption compared to MOSFET, higher efficiently and P-CNFET and N-CNFET, which having the same device geometries and mobilities and subsequently, the same current drive abilities, essential for transistorsizinginthe complex circuits[4-6].

This paper presents a CNFET programmable frequency divider that composed of 3 Double Edge Triggered Flip-flop (DET) and multiplexer 2:1 with division ratios 2 or 3 and duty-cycle about 50% at the output signal.

The rest on the paper is organized as follows: in Section2, a brief review of the CNFET technology is presented. The proposed programmable frequency divider is explained inSection 3.The simulation results and comparisonsare presented in Section 4and Section5concludesthepaper.

II. CARBON NANOTUBE FIELD EFFECT TRANSISTOR

A CNFETs which used Carbon Nanotubes (CNTs) for channel of a transistor, can be made of metal or semiconductor, based onitschiralityvector,identified by(n1,n2) shows, the arrangement angle of its carbon atoms across the nanotube must be specified If n1,n2=3k(k ∈ Z), the CNFETs are conducting and otherwise they are semi conducting [4, 7].

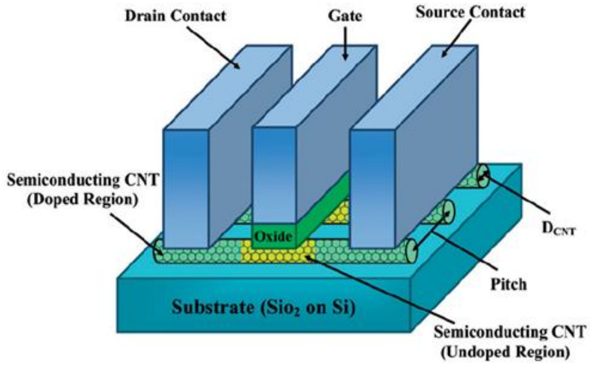


Fig.1. Schematic diagram of a CNFET

Figure 1 [4] illustrates the schematic of a typical CNFET device. The distance between the centers of two

International Journal of Electronics Communication and Computer Engineering
Volume 5, Issue 4, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

adjoining CNTs under the same gate of a CNFET is named pitch. The approximate width of the gate of a CNFET can be estimated using the following (1)[4, 8]

$$w_{gate} \approx Min(w_{\min}, \mathrm{N} \times \mathrm{pitch}) \quad (1)$$

In upon equation, Wmin is the minimum width of the gate and N is the number of nanotubes under the gate. Like a MOSFET device, a CNFET has also threshold voltage required the voltage to turn on the device electrostatically through the gate. A great noticeable to CNFET is that its threshold voltage (Vt)is able to be modified via changing the diameter of its CNTs. This feature makes CNFET more flexible than MOSFET for designing digital circuits. The half band gap of a CNFET almost considered as the threshold voltage of a CNFET and can be estimated by the following (2)[4, 8]:

$$v_{th} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{a v_{\pi}}{D_{CNT}} \approx \frac{0.43}{D_{CNT}\ (\mathrm{nm})} \quad (2)$$

Wherethe parameter e is the unit electron charge and a is the carbon-to-carbon atom distance and about (0.249nm), V_{π} (3.033eV) the carbon– bond energy in the tight bonding model and D_{CNT} is the diameter of CNT, calculated by the following (3) [4] It can be concluded from Equation (2) that the threshold voltage of the CNFET is an inverse function of the diameter of CNT.

$$D_{CNT} = \frac{a \times \sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \approx 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (3)$$

Because of the more similarities between CNFETs and MOSFETs in phrases of features and operation, CNFET is applied for thepresented circuit.

III. Proposed Frequency Divider

In this section, CNFET-based programmable frequency divider is presented. This frequency divider which is shown in Figure 2 composed of 3 Double Edge Flip-Flop (DET sample data by both the clock rising edge and falling edge) and a 2:1 multiplexer (MUX).

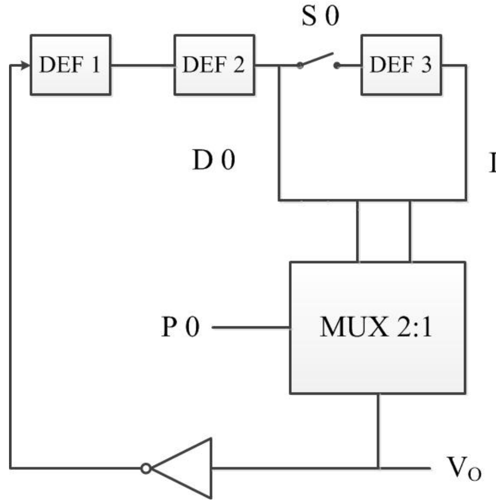


Fig.2. The Proposed CNFET –based Programmable Frequency Divider

After second DET, 2 outputs were taken all of which were connected to a 2:1 MUX. After first of these outputs, a switch (made with N-type transistor) was placed between 2 DET final to decrease loading effect. By getting from these switch and selector inputs of MUX can be determined the division ratios 2 or 3 appeared in the output. The output of MUX that is also the output of the frequency divider connected to a NOT gate that the output of NOT gate is the input of first DET.

The performance of the circuit is in the way that, based on which of these division ratios 2 or 3 came into consideration, the selector inputs of mux should have specific quantity, and according to desire division ration, states (on or off)of switch change.

Circuit of CNFET-based Double Edge Flip-Flop shown in Figure 3 ([9]reported this circuit with CMOS technology). The input signal of the proposed design is CLK in this figure.

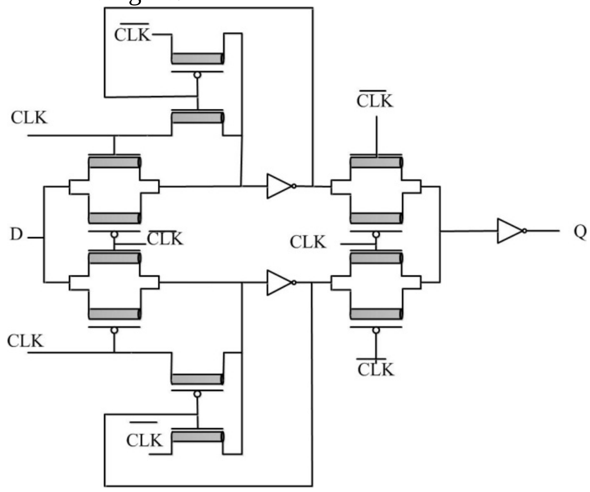


Fig.3. CNFET-based DET flip-flop

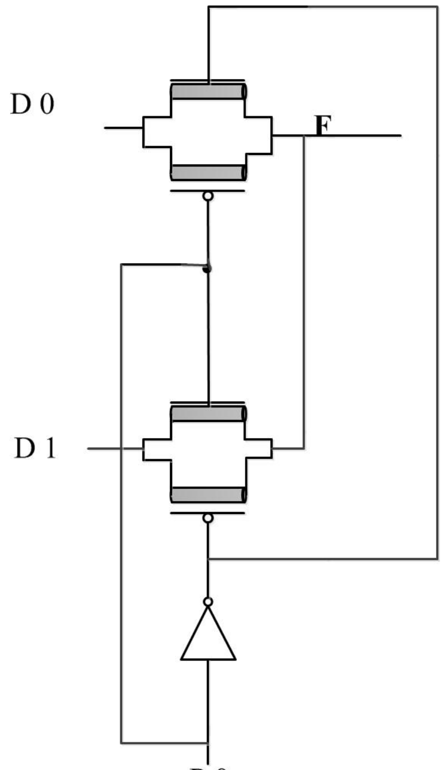


Fig.4. CNFET-based 2:1 MUX

International Journal of Electronics Communication and Computer Engineering
Volume 5, Issue 4, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

Circuit of CNFET 2:1 MUX that based on Transmission gates shown in Figure 4.

($D_{0,}D_1$) are the out puts of Flip-flops those also are inputsMUX and F is also MUX output that is linked to the first DET through a NOT gate.

Table 1 illustrated the plan of proposed frequency divider programmability. (P_0) are the selector inputs of the MUX and (S_0) is the switch.

Table1: Divide algorithm

Division ratio	2	3
P_0	0	1
S_0	OFF	ON

The input signal of the proposed design is shown in Figure 5.

The output signals of the proposed design with a 1GHz input signal in division ratios 2 or 3 respectively shown in Figure 6.

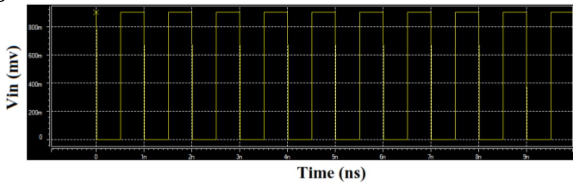
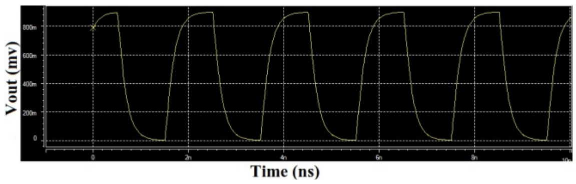
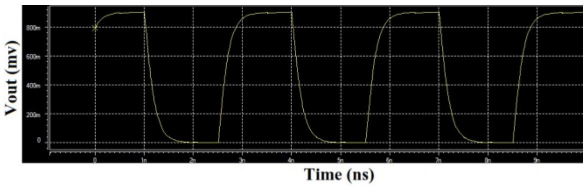


Fig.5. Input signal of the proposed Frequency Divider



(a)



(b)

Fig.6. Output signals of the proposed programmable Frequency divider with division ratios a) 2 b)3

IV. Simulation Result and Comparison

This work is simulated using Synopsys HSPICE 2008 simulator with the Compact SPICE Model[10, 11]. For 32nm CNFET-based circuit, including all non-idealities. The parameters of the CNFET model and their values, with short explanations are shown in table2[4, 5].

Table 2: CNFET model parameters

Parameter	Description	Value
L_{ch}	Physical channel length	32nm
L_{geff}	The mean free path in the intristic CNT channel	100nm
L_{ss}	The length of doped CNT source-side extension region	32nm
L_{dd}	The length of doped CNT drain-side extension region	32nm
k_{gate}	The dielectric constant of high-k top gate dielectric material	16

The delay of each circuit is determined from the time that the input signal reaches 0.5 V_{DD} of the time that the output signal reaches the same voltage level.

The average power consumption throughout Transition time (20 nsec) is also regarded as the power consumption parameter. The performance of the circuits can be considered by calculating PDP, to produce a compromise between the power consumption and the delay of the circuits, which is the multiplication consequence of the average power consumption and the maximum delay.

The circuit is simulated at 0.9V supply voltage and at 1GHz frequency with the 15fF output load capacitor. The detailed results of this simulation arelistedinTable 3.

Table 3: The result of the experiment

Division ratio	Power $(\times 10^{-6}W)$	Delay $(\times 10^{-9}s)$	PDP $(\times 10^{-15}J)$
2	61	1.640	100.04
3	62	2.640	163.68

The simulation results for comparing the proposed circuit with the other frequency divider circuits are listed in table 4. (The power that reports in this table for proposed frequency divider is the maximum power average of all division ratios). based on the simulation results the proposed design hassuperior performance.

Table 4: Report and comparison of the proposed work and the previous work

Frequency divider	Division ration	Technology	Frequency (GHz)	Power (mW)
[12]	128,129	0.7um	1.75	24
[13]	32,33	0.35um	3	27
[14]	220-224	0.25um	5.5	59
[15]	8,9	0.18um	1-4	3.3
[16]	55,56	0.18um	3.2-6.1	4.6
[17]	8,9	0.25um	1.8-2.4	24
[18]	32,33, 47, 48	0.18um	2.4-2.484	2.2
Proposed (CMOS)	2,3	0.18-um	1	10
Proposed (CNFET)	2,3	32-nm	1-2	0.07

V. Conclusion

This paper presents a Carbon Nanotube Field Effect Transistor (CNFET)-based programmable frequency divider composed of 3 Double Edge Flip-Flops and a 2:1 multiplexer with division ratios 2 or 3. The major characteristics of this frequency divider are the different division ratios which programmable with switch and selector inputs of multiplexer and the output signal which has about 50% Duty-cycle at the output voltage. HSPICE based on CNFET model used to produce simulation results for this work. At 0.9 V supply voltage; power consumption for proposed frequency divider is 0. 07mW. The Simulation results show high performance compared to other frequency dividers.

International Journal of Electronics Communication and Computer Engineering
Volume 5, Issue 4, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

REFERENCES

[1] S. Saeedi, M. Atarodi, and M. S. Bakhtiar, "A divide-by-3 frequency divider for I/Q generation in a multi-band frequency synthesizer," in *Circuits and Systems, 2008. APCCAS 2008. IEEE Asia Pacific Conference on*, 2008, pp. 1383-1386.

[2] M. Alioto, R. Mita, and G. Palumbo, "A Design Methodology for High-Speed Low-Power MCML Frequency Dividers," in *Electronics, Circuits and Systems, 2006. ICECS '06. 13th IEEE International Conference on*, 2006, pp. 1308-1311.

[3] M. Zhang, S. K. Islam, and M. R. Haider, "Efficient driving-capability programmable frequency divider with a wide division ratio range," *Circuits, Devices & Systems, IET,* vol. 1, pp. 485-493, 2007.

[4] M. H. Moaiyeri, R. F. Mirzaee, K. Navi, and A. Momeni, "Design and analysis of a high-performance CNFET-based Full Adder," *International Journal of Electronics,* vol. 99, pp. 113-130, 2012.

[5] M. H. Moaiyeri, R. Chavoshisani, A. Jalali, K. Navi, and O. Hashemipour, "High-performance mixed-mode universal min-max circuits for nanotechnology," *Circuits, Systems, and Signal Processing,* vol. 31, pp. 465-488, 2012.

[6] G. Cho, Y.-B. Kim, F. Lombardi, and M. Choi, "Performance evaluation of CNFET-based logic gates," in *Instrumentation and Measurement Technology Conference, 2009. I2MTC'09. IEEE*, 2009, pp. 909-912.

[7] S. Lin, Y.-B. Kim, and F. Lombardi, "A novel CNTFET-based ternary logic gate design," in *Circuits and Systems, 2009. MWSCAS'09. 52nd IEEE International Midwest Symposium on*, 2009, pp. 435-438.

[8] Y. B. Kim, Y.-B. Kim, and F. Lombardi, "A novel design methodology to optimize the speed and power of the CNTFET circuits," in *Circuits and Systems, 2009. MWSCAS'09. 52nd IEEE International Midwest Symposium on*, 2009, pp. 1130-1133.

[9] M. Pedram, Q. Wu, and X. Wu, "A new design of double edge triggered flip-flops," in *Design Automation Conference 1998. Proceedings of the ASP-DAC'98. Asia and South Pacific*, 1998, pp. 417-421.

[10] J. Deng and H.-S. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part II: Full device model and circuit performance benchmarking," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 3195-3205, 2007.

[11] J. Deng and H.-S. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: Model of the intrinsic channel region," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 3186-3194, 2007.

[12] J. Craninckx and M. S. Steyaert, "A 1.75-GHz/3-V dual-modulus divide-by-128/129 prescaler in 0.7-µm CMOS," *Solid-State Circuits, IEEE Journal of,* vol. 31, pp. 890-897, 1996.

[13] S. Levantino, L. Romanò, S. Pellerano, C. Samori, and A. L. Lacaita, "Phase noise in digital frequency dividers," *Solid-State Circuits, IEEE Journal of,* vol. 39, pp. 775-784, 2004.

[14] N. Krishnapura and P. R. Kinget, "A 5.3-GHz programmable divider for HiPerLAN in 0.25-/spl mu/m CMOS," *Solid-State Circuits, IEEE Journal of,* vol. 35, pp. 1019-1024, 2000.

[15] X. P. Yu, A. Do, W. M. Lim, K. S. Yeo, and J.-G. Ma, "Design and optimization of the extended true single-phase clock-based prescaler," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 54, pp. 3828-3835, 2006.

[16] X. Yu, W. Lim, M. Do, X. Yan, and K. Yeo, "6.1 GHz 4.6 mW CMOS divide-by-55/56 prescaler," *Electronics Letters,* vol. 44, pp. 1402-1403, 2008.

[17] H. JOshi and S. M. Ranjan, "A 1.8 GHz-2.4 GHz fully programmable frequncy divider and dual-modulus prescaler for high speed frequency operation in PLL system using 250 nm CMOS technology," *International Journal of Engineering Research and Applications,* vol. 2, pp. 1510-1517, 2012.

[18] V. K. Manthena, A. Do, C. C. Boon, and K. S. Yeo, "A Low-Power Single-Phase Clock Multiband Flexible Divider," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on,* vol. 20, pp. 376-380, 2012.

AUTHOR'S PROFILE

Afshin Kadivarian
was born in Kermanshah, Iran in 1987. He received B.Sc. degree in electronic engineering from Islamic Azad University of Kermanshah, Iran, in 2010 and M.S. degree from Science And Research Branch, Islamic Azad University, Tehran, Iran in 2014.His principle research interests include digital signal processing, FPGA design, VHDL, very large scale integration (VLSI) and carbon nanotube field effect transistor (CNFET). A. kadivarianisa member of Young researchers club, Scienc and research branch, Islamic Azad university, Tehran, Iran.
Email: afshin_kadivaryan@yahoo.com