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Study, Implementation and Comparison of Different Array Multipliers using Modified Shannon Based Adder Cell

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***Abstract* – For a longer battery life a device with less power consumption is desired. Multiplier is the basic component of mostly digital systems so a multiplier with low power dissipation and less area is desirable. In this paper Carry save array (CSA) array multiplier is designed using Modified Shannon based adder cell and compared with other existing work in terms of power dissipation. The parameters are analyzed using BSIM4 model at 90nm deep submicron technology. The schematic is developed using DSCH 3.1 CAD tool and layout is generated using Microwind 3.1 CAD tool. The Modified Shannon based adder cell is optimized using transistor sizing technique. The CSA multiplier shows better performance with optimized modified Shannon based adder cell.**

***Keywords* – Shannon adder, CSA, DSP, Multiplier, Power.**

I. INTRODUCTION

In arithmetic computing system multiplication is the fundamental operation which is used in many DSP applications such as convolution, Fast Fourier Transformation (FFT), filtering and ALU of computer system. Since every digital system needs high speed so a fast computing multiplier is always desired. The processing speed of arithmetic circuit mainly depends upon the multiplication time. Now a day's every device is becoming portable so multimedia and portable devices are dominating the whole market. All of such devices consist of some processor which contains units like DSP and ALU for computation etc. All of these units require computational units like adder and multiplier. Since in VLSI power, area and speed are the main design constraints so the scope of research for an efficient multiplier is always high. For a long battery life power consumption must be reduced [1] This paper presents the study of carry save array multiplier based on modified Shannon based adder cell in terms of power consumption and area required.

Digital multiplier is a very important component of any digital system which is used for implementing arithmetic operations. Depending upon the application various multipliers can be utilized. The type of multiplier depends upon the arrangement of the components in the configuration of the multiplier. The efficiency of the multiplier determines the efficiency of the processor. Various configurations of multipliers like serial-parallel array multipliers are involved to improve the performance in terms of power, area and delay. Low power design with high speed of operation is more essential. Array multipliers as CSA (carry save array) are discussed in section II. The modified Shannon based adder cell is discussed in section III.

II. SHANNON THEOREM

According to the Shannon theorem if any logical Boolean expression have many binary variables such as $f(b_0, b_1, b_2, b_3, ...b_i ....., b_n)$ then this expression can be divided in two terms. For first term a particular variable b_i set as 1 and multiplied with the expression and again for the second term set the particular variable b_i as 0 and multiply with the compliment of the variable to the expression as

$$f(b_0, b_1, b_2, b_3, ...b_i ....., b_n) = b_i f(b_0, b_1, b_2, 1..., b_n)' + b_i' f(b_0, b_1, b_2, 0..., b_n)' \quad (1)$$

The theorem is repeated for each variable until the full reduction is achieved. A Shannon theorem is very useful for multiplier and pass transistor logic circuits. Shannon theorem is applied to the logical function using n-1 variables as the control input and three data lines are set to logic1.These source inputs are connected to VDD lines which are connected to ground.[1].The remaining nth variable is connected from data input to the source input. In the array the direction of flow of data is horizontal and for control signal is vertical. At the intersections n type transistors are connected and the transistors which are canceling each other get removed.

III. ADDER ARCHITECTURE

The adder used to implement CSA is modified Shannon based adder cell which combines the MCIT technique for sum and used Shannon theorem for carry circuit. An input B and B` are used as the control signal of the sum circuit [6].

Sum = (A xor B)C`+(A xor B)`C (2)

The sum circuit has no of transistor count as six. The C and C` are differential nodes of the circuit. For carry circuit the Shannon theorem is applied and the modified expression for carry is

Carry = (A xor B)`B+(A xor B)`C (3)

By using the Shannon theorem the sum and carry expressions are condensed and the no of transistors with area and power consumption also get reduced [2]. Since the no of transistor count for carry circuit is only two. In this paper array multiplier is designed using modified Shannon based adder cell and compared in terms of power dissipation. Figure.1 shows a modified Shannon based adder cell which consist of six transistors for sum circuit and two transistors for carry circuit.

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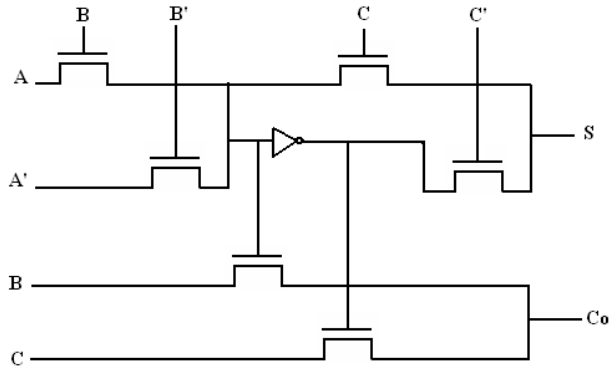

Fig.1. Modified Shannon Based Adder Cell

IV. Array Multiplier

An array multiplier consists of an array of full adder and half adder and it used in different data path circuits. In array multiplier by using the AND gate the partial product terms are simultaneously generated and applied to the adder array. There are different types of the array multipliers like CSA, Braun and Baugh Wooley multipliers. In this paper 8x 8 bit carry save array multiplier is designed using optimized modified Shannon based adder cell and different adder cells as CMOSFA,CPL,HYBRID adder cell[3]-[7]using 90 nm technology.

A. Carry saves array multiplier

This array multiplier is a fast and linear multiplier in which instead of ripple carry adder, Carry save adder is used for adding each group of partial product terms as RCA is a very slow adder. The partial product addition is carried out in carry save form. The final addition is done by using ripple carry adder. An n-bit carry save adder consist of n disjoint full adders. The adder has three n-bit inputs and two n-bit outputs as sum and carry. Since there is no carry propagation within the individual adder the speed of carry save array multiplier is very high. As the linear propagation of data is used in CSA multiplier the size of array increases with the increase of operand in square manner. The length of array depends upon the multiplier and the width of the row depends upon the size of multiplicand.Figure.2 shows a 4*4 bit carry save array multiplier.

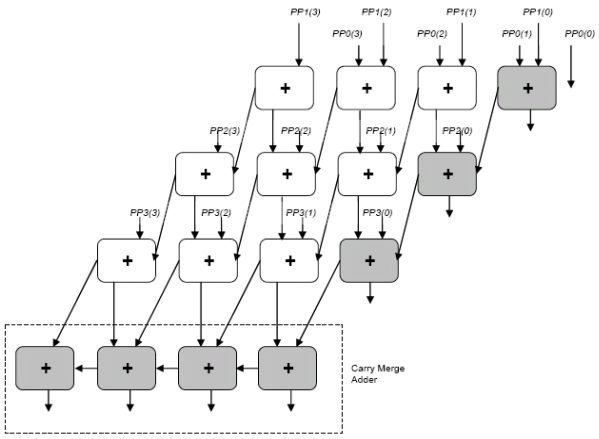

Fig.2. Carry Save Array multiplier

V. Results and Discussions

Since the critical path contains sum and carry signal so a full adder with balanced sum and carry delay is desirable. A large array multiplier has high speed and low power. Using BSIM4 model the parameters of 8x8 bit multiplier are analyzed. In this paper CSA multiplier is designed using optimized modified Shannon based adder cell and compared with other existing work. The width of transistor is varied from 2µm to 100 nm.

Table I: Comparison of 8x8 bit Array Multiplier for Power dissipation

Multiplier type	Adder cell type	Power(mW) (With optimization)	Transistor count
CSA	CMOSFA	0.9	28x64
	CPL	1.3	32x64
	HYBRID	0.12	14x64
	MODIFIED SHANNON	0.05	8x64

Table-I shows the comparison between multiplier using different adder cells in terms of power dissipation. Due to less transistor count and less critical path CSA multiplier using modified Shannon based adder cell have lesser power dissipation. Due to regular structure of array the CSA multiplier uses lesser no of transistor count.

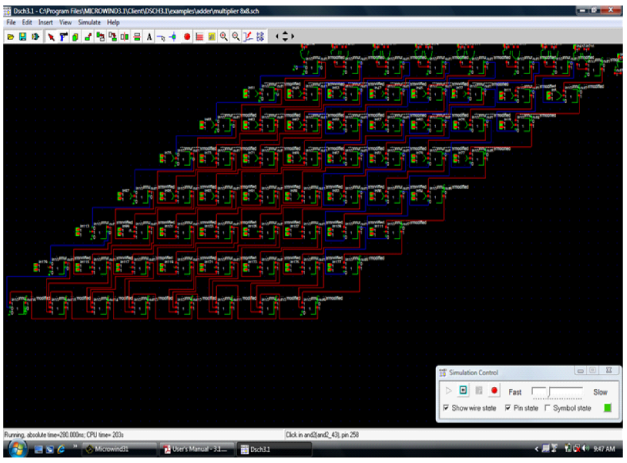

Fig.3. Schematic of 8x8 bit CSA Multiplier

In the first phase the modified Shannon based adder cell is designed and analyzed using BSIM4 Analyzer then the 8 bit carry save array multiplier is designed and compared using this adder cell and other existing adder cells as CMOSFA,CPL,SFA,HYBRID Full Adder. Among all adders modified Shannon based adder gives the best performance in terms of power dissipation. The functionality of the circuit is analyzed using all input combinations. Fig.3 shows the schematic of the 8 bit CSA multiplier which is created using DSCH3.1 CAD tool

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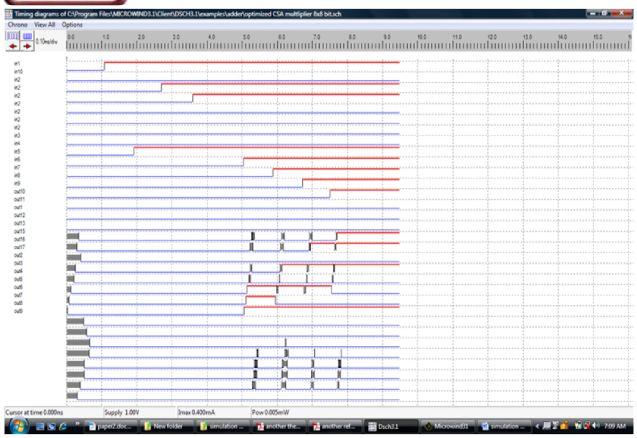

Fig.4. Simulation of 8 bit CSA multiplier using modified Shannon based adder

Fig.4 shows the simulation of CSA multiplier using modified Shannon based adder cell. The power dissipation is calculated by using DSCH3.1 CAD tool. Fig.5 shows the Comparison chart of the performance of CSA multiplier using different adder cell. Chart shows that modified Shannon based adder gives the least power dissipation which is required for a longer battery life. Fig.6 shows the layout of 8x8 bit CSA multiplier. The layout shown in the Figure.6 is generated using Microwind 3.1 VLSI CAD tool. Due to lesser no of transistor required the multiplier occupies the small area also.

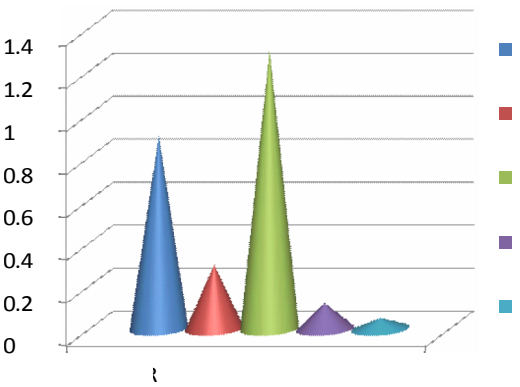

Fig.5. Comparison chart of the performance of CSA multiplier using different adder cell for power dissipation

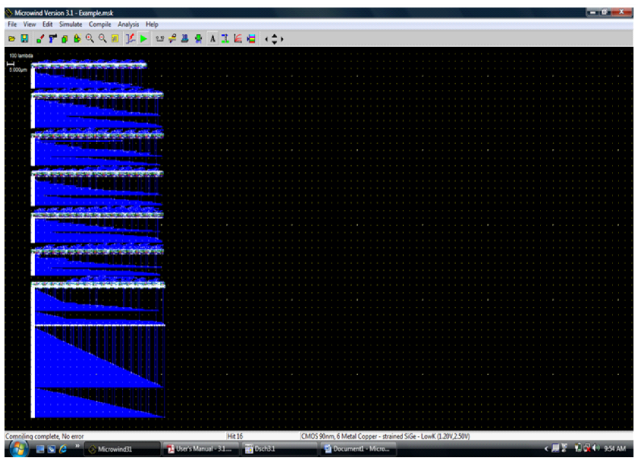

Fig.6. Layout of CSA Multiplier

VI. Conclusion

For a computational circuit like ALU and DSP processors the multiplier is an important component which must occupy less area and have less delay with low power dissipation. In this paper carry save array multiplier was designed using existing adders and simulated in 90 nm technology with BSIM4analyzer.Five different adders were used to design 8x8 bit carry save array multiplier and compared with each other in terms of power dissipation. Modified Shannon based adder shows less power dissipation than others.

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