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Importance of Low Power Application Memory Cell in CMOS Design

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Abstract – **The criterion for memory which is essential in all digital system is efficiency of the memory array i.e number of store data bits per unit area, the time require to store and/or retrieve particular data bits in the memory, high density, high throughput etc. The memory array design using shift registers is the option for high throughput, high density with simple circuit structure for large scale digital system. This paper represent some literature survey on design and study of different methods proposed by different authors.**

Keywords – **Low Power Application Memory Cell in CMOS Design, Shift Registers.**

I. Introduction

The memory array capable of storing large quantity of digital information essential in all digital system. The amount of memory required in system depends on the type of application but the major criterion for memory which is essential in all digital system is efficiency of the memory array i.e number of store data bits per unit area, the time require to store and/or retrieve particular data bits in the memory, high desity, high throughput etc. The ever increasing demands for large data storage capacity, high throughput ,speed, has driven the fabrication technology and memory development towards more compact design rules. Also the static and dynamic power consumption of the memory array is a significant factor to be consider in the design because of the increasing imporatance of low power application. VLSI design in the late CMOS era is driven by an ever-increasing challenge to cope with unreliable components at the device, circuit, and system levels. Reliability challenges include bias temperature instability, dielectric breakdown, early-life failure, and soft errors, as well as their interaction with statistical process variation. Design and test solutions at the different node and beyond need to resolve these reliability issues.

II. Literature Survey

From the rigorous review the survey of Kiyoo Itoh presented history of Dynamic random-access memory (DRAM) has been the only high-density RAM used for over 30 years despite many attempts to replace it. Still contributing to IT advances, it has achieved an unprecedented six fold increase in memory capacity in the last three decades, from the 1-Kbit level in 1970 to the 1- to 4- Gbit level today, as shown in Figure 2.1 . Such rapid progress, however, would have been impossible without the implementation of many inventions and innovative technologies and the efforts of many talented people. The one-transistor one-capacitor cell (the 1- T cell) invented by Robert Dennard, and supported by his scaling theory.

The first production of semiconductor memory announced by Intel and IBM in 1970. Had a profound impact on his research at Hitachi Ltd. On the side, he brought the hottest DRAM samples and evaluated them to judge how DRAMs would impact Hitachi mainframe computers, while still being involved in magnetic memory device/system design. Eventually, however, he was forced to change his research field from magnetic thin-film memory to semiconductor memory. This change was so exceptionally sudden and difficult, He felt like a victim of fate. Looking back however, He realizes how fortunate He was to have witnessed such an advancement of DRAMs.

This paper investigated the architecture design of 3D integrated DRAM using wafer-level 3D integration technology. The key is to focus on coarse-grained inter-sub- array 3D memory partitioning in order to accommodate the potentially significant pitch mismatch between DRAM word-line/bit-line and TSVs. Two inter-sub-array 3D partitioning approaches are presented, targeting different TSV complexity vs. memory access energy trade-offs. Moreover, an inter-die inter-sub-array redundancy repair approach has been proposed to improve the 3D DRAM redundancy repair efficiency. CACTI 5 has been modified to evaluate the proposed 3D partitioning strategies, and estimation results show encouraging performance advantages over direct 3D die packaging and conventional 2D design. Finally, a memory redundancy repair simulator has been developed to demonstrate the higher repair success rate achieved by the proposed inter-die inter-sub-array redundancy repair approach.

This paper presented by Takayasu SAKURAI, Kazutaka NOGAMI, Kazuhiro SAWADA, and Tetsuya IIZUKA (CH2584-1/88/0000-0014 $1.00 0 1988 IEEE). Transparent-Refresh DRAM (TReD) is proposed to realize a fast and high-density 'static' RAM. The TReD uses dual-port DRAM cells, in which one port is assigned exclusively for a refresh operation and the other port for a normal read-right operation. Key design considerations were discussed in detail. A test device was successfully fabricated using 1.2p-1 double-AI double-poly CMOS technology, and the feasibility was verified. The TReD can provide very high-density static RAMs and is suitable for a RAM macro in ASIC environments. This paper proposes a new approach to a virtually static RAM, namely Transparent-Refresh DRAM (TReD). Using dual-port DRAM cells, the TReD provides both of the high-density feature and the fast memory access time. The memory cell size of the TReD is smaller than the conventional SRAM and the access speed is faster than that of the PSRAM and the VSRAM. This is because, in the TReD, the internal refresh takes place completely in parallel with the normal operation as a background job, thanks to the dual port configuration.

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The RAM is suitable for a RAM macro I ASIC environments, where critical timing control of a refresh is impossible because of a CAD limit. The new work on DRAM presented by Hajime Furusawa, Shinichiro Nogami, Takahisa Ogawa, Masanobu Kumazaki, Naoki Okada and Hiroyuki Yamamoto. In this paper, author developed high-performance peripheral transistors using 95nm DRAM process without any costly approaches. DPS became 10ps/stage faster in the evaluation extracted from the ring oscillator TEG. Estimated DPS would be 15ps/stage (Vcc=1.8V) without load capacitance. Although high performance was accomplished, the data retention time was degraded, mainly due to thin selective EPI. In effect, the retention time requirement would not be so strict in the embedded solution. Depending on the architecture and customer demand. In order to improve data retention time performance, a dual-EPI growth process was developed and evaluated. Parametrically, the dual-EPI process shows excellent results, but has not yet been properly optimized to get good yield. The dual-EPI process is in the development stage, which is very unique and beneficial for future device applications.

Michael Powell, Se-Hyun Yang, Babak Falsafi, Kaushik Roy, Senior Member, IEEE, and T. N. Vijaykumar present a paper on Reducing Leakage in a High- Performance Deep-Submicron Instruction Cache Deep-submicron CMOS designs maintain high transistor switching speeds by scaling down the supply voltage and proportionately reducing the transistor threshold voltage. Lowering the threshold voltage increases leakage energy dissipation due to sub threshold leakage current even when the transistor is not switching. Estimates suggest a five-fold increase in leakage energy in every future generation. In modern micro architectures, much of the leakage energy is dissipated in large on-chip cache memory structures with high transistor densities. While cache utilization varies both within and across applications, modern cache designs are fixed in size resulting in transistor leakage inefficiencies.

This paper explores an integrated architectural and circuit-level approach to reducing leakage energy in instruction caches (i-caches). At the architecture level, we propose the Dynamically Resizable i-cache (DRI i-cache), a novel i-cache design that dynamically resizes and adapts to an application ' s required size. At the circuit-level, we use gated- , a novel mechanism that effectively turns off the supply voltage to, and eliminates leakage in, the SRAM cells in a DRI i-cache ' s unused sections. Architectural and circuit-level simulation results indicate that a DRI i-cache successfully and robustly exploits the cache size variability both within and across applications. Compared to a conventional i-cache using an aggressively-scaled threshold voltage a 64 K DRI i-cache reduces on average both the leakage energy-delay product and cache size by 62%, with less than 4% impact on execution time. Our results also indicate that a wide NMOS dual- gated-transistor with a charge pump offers the best gating implementation and virtually eliminates leakage energy with minimal increase in an SRAM cell read time area as compared to an i-cache with an aggressively-scaled threshold voltage.

This paper describes the Dynamically Resizable instruction cache (DRI i-cache). The key observation behind a DRI i-cache is that there is a large variability in i-cache utilization both within and across programs leading to large energy inefficiency for conventional caches in deep-submicron designs; while the memory cells in a cache' unused sections are not actively referenced, they leak current and dissipate energy. A DRI i-cache ' s novelty is that it dynamically estimates and adapts to the required i-cache size and uses a novel circuit-level technique, gated- [18], to turn off the supply voltage to the ache ' s unused SRAM cells. In this section, we describe the anatomy of a DRI i-cache. In the next section, we present the circuit technique to gate a memory cell ' s supply voltage.

III. Conclusion

After this survey one important paper which work I want to continues that Xiaoyao Liang Harvard University Ramon Canal Universitat Polite`cnica de Catalunya Technology an scaling promises increasing transistor density and increasing performance in microprocessors. However, the road toward this promise is fraught with difficulties resulting from increased process variations that limit performance gains and affect the stability of key circuit blocks such as on-chip memories. Addressing these problems requires innovation at all levels in the design flow— from devices to system architecture. Fluctuations in device channel dimensions and dopant concentrations are two forms of process variation that affect circuit performance. Gate length variation can change the transistor ' s effective driving capability and the threshold voltage due to short channel effects. Random dopantq1a variations also change each device's threshold voltage.

IV. References

[1] G. Eneman, P. Verheyen, A. De Keersgieter, M. Jurczak, and K. De Meyer, " Scalability of stress induced by contact-etch-stop layers: A simulationstudy, " IEEE Trans. Electron Devices , vol. 54, no. 6, pp. 1446–1453, Jun. 2007.

[2] C. Hess, S. Saxena, H. Karbasi, S. Subramanian, M. Quarantelli, and A. Rossoni et al. , " Device array scribe characterization vehicle test chip for ultra fast product wafer variability monitoring, " in Proc. Int. Conf. Microelectron. Test Struct Tokyo, Japan, 2010, pp. 145–149.

[3] M. Yabuuchi, K. Nii, Y. Tsukamoto, S. Ohbayashi, S. Imaoka, and H. Makino et al. , " A 45 nm low-standby-power embedded SRAM with improved immunity against process and temperature variations, " in Proc. IEEE Int. Solid-State Circuits Conf. , 2007, pp. 326–328.

[4] H. Pilo, C. Bardwin, G. Braceras, C. Browning, S. Lamphier, and F. Towler, " An RAM design in 65-nm technology node featuring read and write-assist circuits to expand operating voltage, " IEEE J. Solid State Circuits , vol. 42, no. 4, pp. 813–819, Apr. 2007

[5] A. Cathingnol, S. Bordez, K. Rochereau, and G. Ghibaudo, " From MOSFET matching test structures to matching data utilization: Not an ordinary task, " in Proc. Int. Conf. Microelectron. Test Struct. , Tokyo, Japan, 2007, pp. 230–233.

[6] S. K. Springer, S. Lee, N. Lu, E. J. Nowak, J.-O. Plouchart, and J. S. Watts et al., Modeling of variation in submicrometer CMOS

ULSI technologies," IEEE Trans. Electron Devices, vol. 53, no. 9, pp. 2168– 2178, Sep. 2006.

[7] R. A. Bianchi, G. Bouche, and O. Roux-dit-Buisson, " Accurate modeling of trench solution induced mechanical stress effects on MOSFET electrical performance, " in IEDM Tech. Dig. , San Francisco, CA, 2002, pp. 117–120.

[8] G. S. May and C. J. Spanos, Fundamentals of Semiconductor Manufacturing and Process Control . New York: Wiley-Interscience, 2006.

[9] F. Boeuf, F. Arnuad, C. Boccaccio, F. Salvetti, J. Todeschini, and L. Pain et al. , " 0.248 µ m2 and 0.334 µ m2 conventional bulk 6T-SRAM bit-cells for 45 nm node low cost—General purpose applications, " in VLSI Symp. Tech. Dig. , 2005, pp.

[10] U. Schaper and J. Eineld, " Parameter variation on chip-level, " in Proc. IEEE Int. Conf. Microelectron. Test Struct. , Apr. 2005, pp. 155–158. [11] P. Friedberg, Y. Cao, J. Cain, R.Wang, and C. Spanos, " Modeling withindie Spatial correlation effects for process-design co-optimization, " in Proc. IEEE Int. Symp. Quality Electron. Des. , 2005, pp. 516–52

[12] H. van der Lann, R. Carpaij, J. Krist, O. Noordman, Y. van Dommelen, and J. van Schoot et al. , " Etch, reticle, and track CD fingerprint corrections with local dose compensation, " Proc. SPIE , vol. 5755, pp. 107–118, 2005.

[13] A. Asenov, A. R. Brown, J. H. Davies, S. Kaya, and G. Slavcheva, " Simulation of intrinsic parameter fluctuations in decananometer M. Orshansky, L. Milor, and . Hu, "Characterization of spatial intrafield gate CD variability, its impact on circuit performance and spatial mask-level correction," IEEE Trans. Semicond. Manuf., vol. 17, no. 1, pp. 2–11, Feb. 2004.

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