International Journal of Electronics Communication and Computer Engineering
Volume 5, Issue 3, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

A Multi Band Low Noise Amplifier as a Front End for Multi-standard Receiver Wireless Network

Shinde Jitendrakumar N.
Associate Professor
ISB&M SOT College of Engineering, Pune
Email: jn_shinde@yahoo.com

Dr. S. K. Bodhe
Director
BoSh Technology, Pune
Email: skbodhe@gmail.com

***Abstract* – The multi-band low noise amplifier can operates on different frequency band. In lower band will works on frequency band 700MHz to 1200 MHz and upper frequency band operates on 1700MHz to 2300MHz.In this external gate source capacitor is used for the input impedance matching. The noise figure is 4.05 and 3.59 for lower and upper band respectively.**

Keywords* – LNA, *Cex1, GATE SOURCE CAPACITANCE, IDCS.

I. INTRODUCTION

With the progress of wireless communications requirements for transceivers that can support multi-bands and multi-standards. The key bottleneck for multiple-standard communications is the implementation of the low- noise amplifier. This can operate at different frequency bands, which plays an important role in the noise performance or sensitivity of the multi-band, multi-standard receiver. The challenges include an input matching, frequency response of power gain, noise figure, and good linearity within the desired bands. A basic approach implements multiple separated narrowband amplifiers, each designed for a different frequency band. Apparently this method undergoes from high power dissipation, a large chip area.

There are three ways of implementing a multi-band LNA. The first way is to use a separate LNA for each standard, resulting in larger die area, higher cost and power. The second way is to use a wideband LNA. It offers the smaller area and power, the sensitivity suffers with large out-of-band unwanted blocker due to the non-linearity of the transistor. The third method is use the concurrent dual-band LNA that offers better trade-off between area, power and sensitivity.

The design of multi-band design of these wide band low noise amplifiers implemented for lower and upper bands. The lower frequency band is from 700MHz to 1200MHz and upper frequency band from 1700MHz to 2300MHz respectively. The main goal of this investigation is to design and implementation of a single reconfigurable multi-band multi-standard low noise amplifier. This low noise amplifier will be designed in such a way that the reconfigurability is achieved by changing of hardware configuration to support these frequency bands. This low noise amplifier is use for the multi-band multi-standard mobile receiver. The multi-band low noise receiver is used an inductively degenerated common source topology. The IDCS topology is cover lower band as well as upper band frequencies. This multi-band low noise amplifier is use the external gate source capacitor. This capacitor is used for the input impedance matching.[1]

The paper is organized as follows: Section I gives introduction information of multi-band low noise amplifier. In the section II we present the design of multi-band low noise amplifier, mathematical calculations and circuit diagram. In section III circuit diagram and simulated results such as scattering parameters, linearity and noise figure calculation are presented. For the purpose of design and implementation we use Agilent's ADS simulator. In Section IV we present the Layout implementation, Simulation and measurement results. In section V we present conclusion and future scope.

II. PROCEDURE

A. *Design of multi-band LNA*

Fig.1 indicates the schematic circuit diagram of multi-band wideband inductively degenerated common source LNA targeted to cover the carrier frequency range from 700 MHz to 1200 MHz for lower band and 1700 MHz a to 2300 MHz for upper band. Multi-band low noise amplifier is used lower values of inductor because it will operate in lower as well as upper band. The external gate source capacitance C_{ex1} and C_{ex2} are the external capacitor required for both the band modes respectively. The external capacitor is used for the input impedance matching. C_{D1} and C_{CD2} are used as load capacitance for lower and upper band respectively. L_G, L_S, L_D, L_l and R_l is the input load inductor and load resistor. [2] [5]

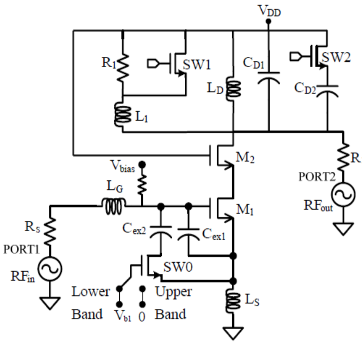


Fig.1. A Schematic Circuit Diagram of Multi-Band Low Noise Amplifier

B. *Design parameter*

For the input impedance matching multi-band low noise amplifier introduce the gate source capacitor *Cex*. The values of capacitors *Cex1* and *Cex2* have to be determined in such a way that the matching conditions for upper band and lower band are fulfilled. Depending of the situation of transistor electronic switch *SW0* whether it is in ON of OFF mode, the LNA will operate either at upper band frequency or lower band frequency. [3]

The following equations are derived for the impedance matching at the input of multi-band low noise amplifier.

i) For upper band mode:

The first transistor *SW0* is off condition.

$$C_{ex} = C_{ex1} = C_{gs\ ex,\ upper\ band}$$

$$Z_{in,upper\ ,band} \approx s(L_G + L_S) + \frac{gm1L_s}{C_{gg1} + C_{gs,upper\ \ band}} + \frac{1}{s(C_{gg1} + C_{gs,upper\ \ band})}$$

$$R_s = \frac{gm1L_s}{C_{gg1} + C_{gs,upper\ \ band}} = 50\Omega$$

ii) For lower band mode:

$$C_{ex} = C_{ex1} + C_{ex2} = C_{gs\ ex,\ lower\ band}$$

$$Z_{in,lower\ \ band} \approx s(L_G + L_S) + \frac{gm1L_s}{C_{gg1} + C_{gs,lower\ \ band}} + \frac{1}{s(C_{gg1} + C_{gs,lower\ \ band})}$$

$$R_s = \frac{gm1L_s}{C_{gg1} + C_{gs,lower\ \ band}} = 50\boldsymbol{\Omega}$$

For the output impedance matching, *SW1* and *SW2* participates important roles in to decide the load at the output. The on and off positions of these switches will set the output impedance matching of the LNA either to operate at upper band or lower band mode.

For the upper band mode *SW1* has to be in ON condition and *SW2* in off condition. In this situation R_1 and L_1 is in series. So to calculate the output impedance matching of low noise amplifier following equations is revised.

For upper band

$$Y_{L\ upper\ \ band} = sC_{D1} + \frac{1}{r + sL_D} + \frac{1}{R_{sw1}R_1 + sL_1}$$

$$Z_{L\ upper\ \ band} = \frac{1}{Y_{L\ upper\ \ band}}$$

$$= \left(\frac{1}{sC_{D1}}\right)(r + sL_D)(R_{upper\ \ band} + sL_1)$$

$$= \frac{R_{upper\ \ band}\, r + s(R_{upper\ \ band}\, L_D + rL_1) + L_1L_Ds^2}{1 + sC_{D1}(R_{upper\ \ band} + r) + s^2C_{D1}(L_1 + L_D)}$$

At lower band mode *SW1* has to be in OFF condition and *SW2* in ON condition. Only R_1 and L_1 are representing the resistance. With the total capacitance $(C_{D1} + C_{D2})$ *and* L_D will set the output impedance matching for lower band mode.

So, for lower band

$$Y_{L\ lower\ \ band} = s(C_{D1} + C_{D2}) + \frac{1}{r + sL_D} + \frac{1}{R_1 + sL_1}$$

$$\therefore\ Z_{L\ lower\ \ band} = \frac{1}{Y_{L\ lower\ \ band}} = \left(\frac{1}{sC_{D,lower\ \ band}}\right)$$

$$(r + sL_D)(R_{lower\ \ band} + sL_1)$$

$$= \frac{R_{lower\ \ band}\, r + s(R_{lower\ \ band}\, L_D + rL_1) + L_1L_Ds^2}{1 + sC_D(R_{lower\ \ band} + r) + s^2C_{D\ lower\ \ band}(L_1 + L_D)}$$

Where

$R_{upper\ band} = R_{sw1} * R_1$ *and* $R_{lower\ band} = R_1$

$C_{D,\ lower\ band} = C_{D1} + C_{D2}$

iii) Calculation of gain of the multi-band low noise amplifier

Gain of upper band

$$S_{21} = 2 \times \frac{v_{out}}{v_{in}}$$

$$S_{21} = GM_{21}(s) \times Z_{L\ upper\ \ band}(s)$$

Gain of lower band

$$S_{21} = 2 \times \frac{v_{out}}{v_{in}}$$

$$S_{21} = GM_{21}(s) \times Z_{L\ lower\ \ band}(s)$$

III. CALCULATION

Now, find out the cutoff frequency

$$\omega = 2\Pi f = 2\Pi \times 2GHz$$

$$= 12.56\ G\ rad/sec$$

The value of L_s is arbitrary value and it should be below 0.55 *nH*. Unnecessary source inductance can lead to LNA oscillations because of gain peaks at higher range frequencies. For this design we assumed the value of 0.55 *nH*.

So we assume *Ls*=0.55 *nH*.

$$\omega_T = \frac{g_m}{(C_{gs} + C_d)} = \frac{R_s}{L_s} = \frac{50}{0.1nH} = 500\ G\ rad/sec$$

The value of Q is given by

$$Q = \sqrt{1 + \frac{1}{p}} \qquad \text{Where } p = \frac{\delta\alpha^2}{5\gamma}$$

The parameters for *p* are dependent on the CMOS technology but typically α is assumed to be 0.8 -1.0 (normally 0.9) δ is set to 2 - 3 times the value of (take to be 4) γ is set between 2 - 3 (normally 2)

$$Q = \sqrt{1 + \frac{1}{p}}$$

$$= 2.67$$

Evaluation of L_G

$$Q = \frac{\omega_0(L_G + L_S)}{2R_s}$$

$$\therefore\ L_G = \frac{2QR_s}{\omega_0} - L_s$$

The source degenerated inductance L_s can be calculated by the following equation:

$$R_s = \frac{g_mL_s}{C_{gs} + C_d} = 50\ \Omega$$

Unnecessary source inductance can lead to LNA oscillations because of gain peaks at higher range frequencies. For this design we assumed the values of 0.55 *nH*.

$$\therefore \; L_G = \frac{2\times 2.67\times 50}{12.56\times 10^9} - 0.55\times 10^{-9}$$

$$= 20.70\ nH$$

Calculation of L_D

$$L_D = \frac{1}{\omega^2 C_L}$$

Assume C_L=100*fF*

L_D =15.60 *nH*

To find gate source capacitance C_{gs}

$$C_{gs\ upper} = \frac{1}{\omega_0^2 (L_G + L_S)}$$

$$C_{gs\ upper} = \frac{1}{(12.56\times 10^9)^2 (21.15\ nH + 0.1 nH)}$$

$$C_{gs\ upper} = 0.298\times 10^{-12} f$$

$$C_{gs\ lower} = \frac{1}{\omega_0^2 (L_G + L_S)}$$

$$C_{gs\ lower} = \frac{1}{(5.93\times 10^9)^2 (43 nH + 0.1 nH)}$$

$$C_{gs\ lower} = 0.6666\times 10^{-15} f$$

Calculation of C_d

$$R_s = \frac{g_m L_s}{(C_{gs} + C_d)} = 50\ \Omega$$

But the transcondutance

$$g_{m\ upper} = \omega_T \cdot C_{gs}$$

$$g_m = 500\times 10^9 \times 0.298\times 10^{-12}$$

$$= 0.149\ mA/V$$

$$g_{m\ lower} = \omega_T \cdot C_{gs}$$

$$g_{m\ lower} = 500\times 10^9 \times 0.666\times 10^{-15}$$

$$= 333.333\ mA/V$$

The above equations show that C_{gs} of lower band is higher than C_{gs} of upper band. Therefore the ending current of low noise amplifier operating at lower band frequency has to be higher than the ending current of the low noise amplifier operating at upper band.

Re-arranging the equation

$$(C_{gs} + C_d) = \frac{g_m L_s}{R_s} = 50\ \Omega$$

$$(0.298\times 10^{-12} + C_d) = \frac{0.00149\times 0.1\ nH}{50}$$

$$\therefore C_d = 295.58\times 10^{-15} f$$

Calculation of dimension of M1

$$W = \frac{3}{2}\frac{C_{gs}}{C_{ox} L_{min}}$$

$$L_{min} = 0.6\times 10^{-6} \quad and\ T_{ox} = 1.01\times 10^{-8}$$

$$\varepsilon_{ox} = \varepsilon_s \varepsilon_0$$

ε_s= a dielectric constant for silicon material =3.9

ε_0=a dielectric constant for the free space =8.85*10^{-12}

So the calculated value of

ε_{ox}=3.9*8.85*10^{-12}

$$C_{ox} = \frac{\epsilon_{0x}}{T_{ox}} = 3.14\times 10^{-3} pF$$

So

$$C_{ox} = 3.14\times 10^{-3} pf$$

$\therefore$ W = 237µm.

Calculation of Q_{in}

$$Q_{in} = \frac{1}{2\omega_o R_s C_{gs} + C_d}$$

$$Q_{in} = \frac{1}{2\times 12.56\times 10^9 \times 50\times (0.298\times 10^{-12} + 295\times 10^{-15})}$$

$$Q_{in} = 2.45$$

Calculation of Gain:

The gain will be calculated by the following equation.

$$G_m = Q_{in}\, g_{m\ upper}$$

$$= 3.65\times 10^{-3}$$

Calculation of $V_{effecive}$

$$V_{effectivev} = \frac{g_m L_{min}}{\mu_n C_{ox} W}$$

μ_n is the device mobility=433cm/V

$V_{effecive}$=*0.717V*

But V_t =*0.67*

So we need to apply total voltage

V=0.717+0.67=1.38V

Noise Figure

$$F_{upper} = 1 + \frac{\gamma}{g_m R_s Q_{in}^2}$$

$$F_{upper} = 1 + \frac{2}{0.00149\times 50\times (2.45)^2}$$

=5.47

$$F_{lower} = 1 + \frac{\gamma}{g_m R_s Q_{in}^2}$$

$$F_{lower} = 1 + \frac{2}{0.333\times 50\times (0.845)^2}$$

=1.17

IV. RESULTS

I) Simulation Results for Lower Band

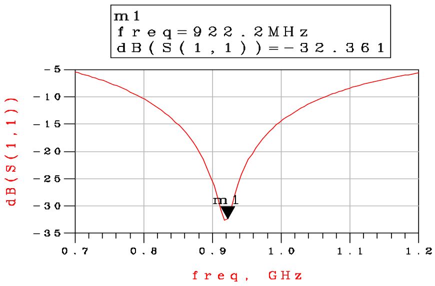


Fig.2. Simulated S_{11} versus frequency

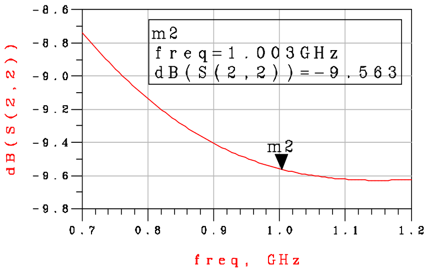


Fig.3. Simulated S_{22} Versus Frequency

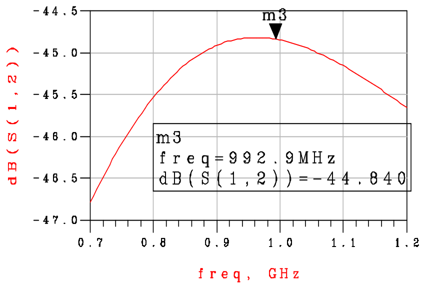


Fig.4. Simulated S_{12} Versus Frequency

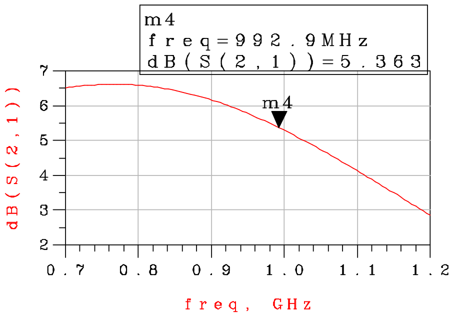


Fig.5. Simulated S_{21} Versus Frequency

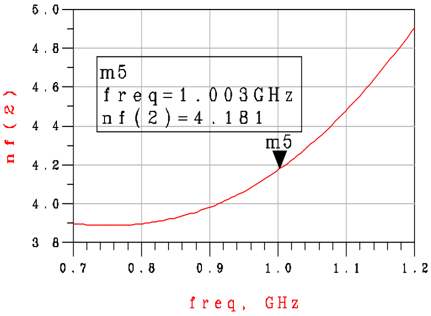


Fig.6. Simulated Noise Figure Versus Frequency

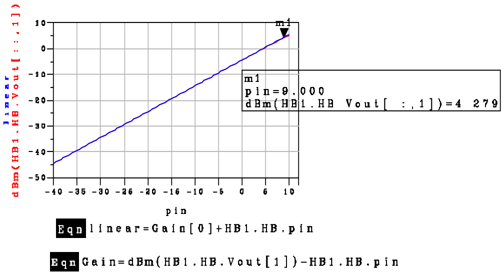


Fig.7. The *IIP*$_3$ of Low Noise Amplifier

The figure for the above simulation results is shown in page no.8 the scattering parameter input reflection coefficient S_{11} measures the input return loss. The input reflection coefficient of this low noise amplifier achieved is -32.361 dB. The scattering parameter output reflection coefficient S_{22} measures the output return loss. The output reflection coefficient of this low noise amplifier achieved is -9.592 dB. The value of about -44.840 at peak frequency and it is a good reverse isolation. S_{21} forward /power gain of low noise amplifier achieved 5.363 dB in the simulation. The simulated noise figure of low noise amplifier is 4.181 dBm. The simulated value of *IIP*$_3$ is 4.279 dBm and it shown in simulated figure. The circuit has been achieved the best value of *IIP*$_3$ with minimum current consumption.[4]

II) Simulation Results for Upper Band

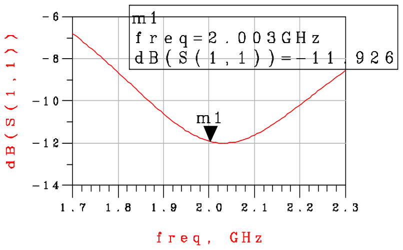


Fig.8. Simulated S_{11} Versus Frequency

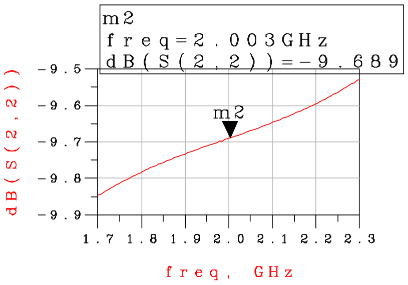


Figure 9: Simulated S_{22} Versus Frequency

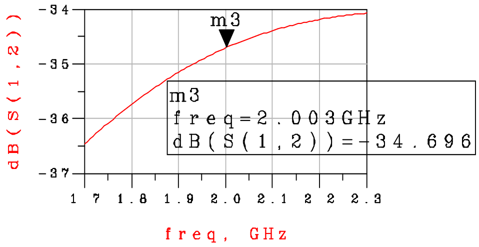


Fig.10. Simulated S_{12} Versus Frequency

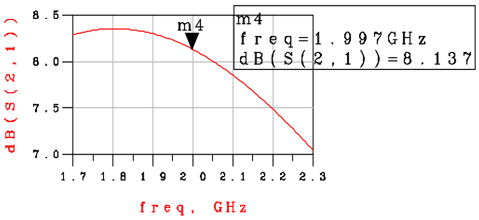


Fig.11. Simulated S_{21} Versus Frequency

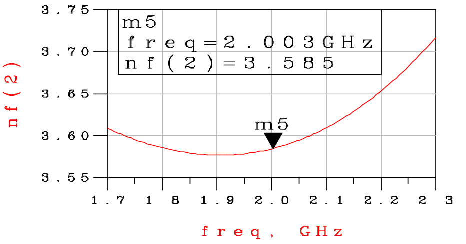


Fig.12. Simulated Noise Figure Versus Frequency

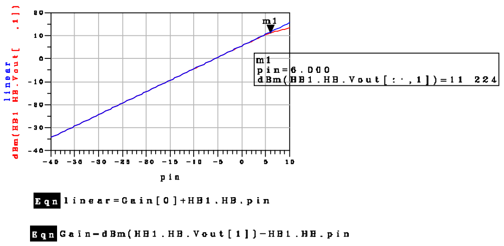
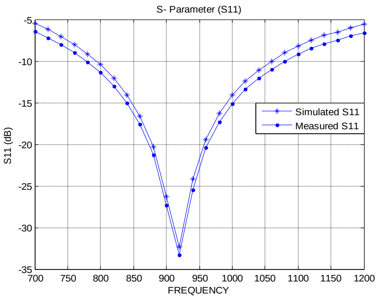


Fig.13. The *IIP*$_3$ of Low Noise Amplifier

The figure for the above simulation results is shown in page no.8. The input reflection coefficient of this low noise amplifier achieved is -11.929 dB. The input reflection coefficient should be below -10dB. The output reflection coefficient of this low noise amplifier achieved is -9.689 dB. Scattering parameters S_{12} i.e. reverse isolation achieved in the simulation. The value of reverse isolation is about -34.696 dB at peak frequency. S_{21} forward /power gain of low noise amplifier achieved in the simulation. The simulation shows that the value of about 8.137 dB. The measured noise figure of low noise amplifier is 3.585 dB. This is between the optimum ranges of low noise amplifier. The simulated value of *IIP*$_3$ is 11.384 dBm and it shown in simulated figure.

III) Comparison Chart of Upper and Lower Band



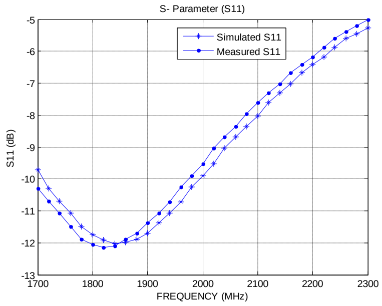


Fig.14. Comparison of S_{11} Versus Frequency For Lower And Upper Band

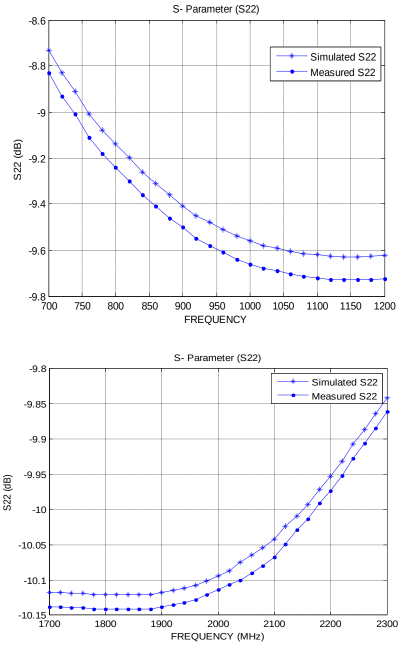


Fig.15. Comparison of S_{22} Versus Frequency For Lower And Upper Band

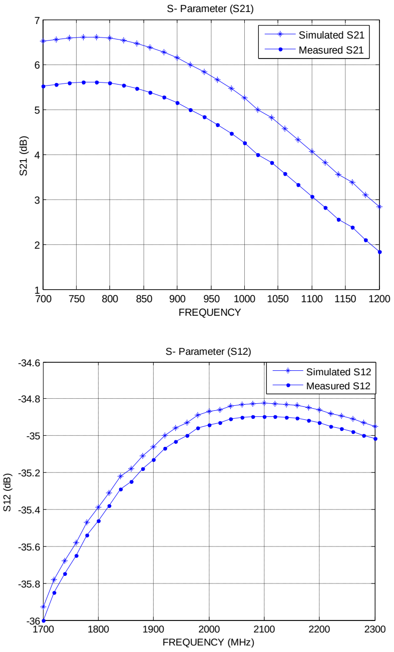


Fig.16. Comparison of S_{21} Versus Frequency For Lower And Upper Band

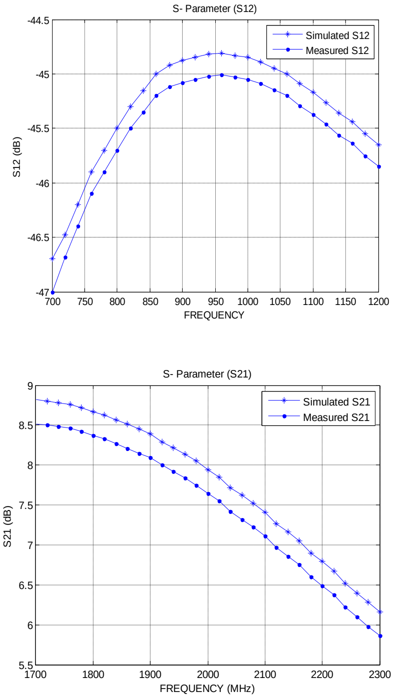


Fig.17. Comparison of S_{12} Versus Frequency For Lower And Upper Band

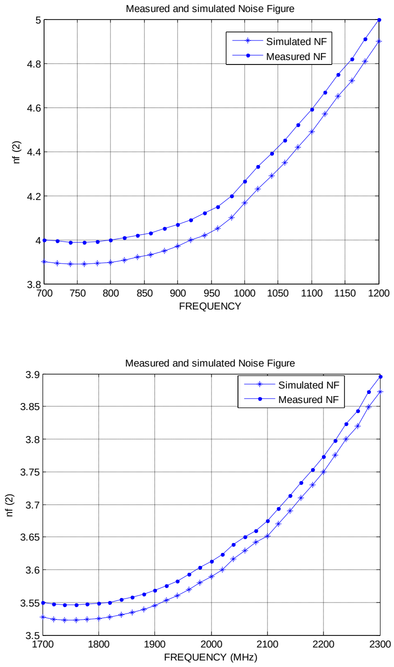


Fig.18. Comparison of Noise Figure Versus Frequency For Lower And Upper Band

The results are divided into two types, simulated and measured as shown figures. The power gain S_{21} for the simulated is about 6.5 dB at the center frequency while for measured gain is about 6.5 dB. The difference between these results is because of the parasitic values of the component. The input return loss for simulation is -32.361 dB and measured input return loss is -11 dB. The difference of simulated and measured is -34.30 dB.

For S_{22} the simulated resulted produced -9.5 dB at the center frequency while without matching network the measured value is -9.7 dB obtained. The reverse isolation S_{12} obtained for simulated value is -45 dB and measured values is -44.7 dB. The noise figure of the schematic circuit is around 4.05 dB at center frequency and measured value is 4.18 dB.

The power gain S_{21} for the simulated is about 8.00dB at the center frequency while for measured gain is about 7.5 dB. The input return loss for simulation is -11.75 dB and measured input return loss is -12.00 dB. The difference of simulated and measured is -0.250 dB.

For S_{22} the simulated resulted produced -10.01 dB at the center frequency while measured value is -10.15 dB obtained. The reverse isolation S_{12} obtained for simulated value is -34.65 dB and measured values is -34.90 dB. The noise figure of the schematic circuit is around 3.59 dB at center frequency and measured value is 3.62 dB.

V. CONCLUSION

The multi-band low noise amplifier can operate at different frequency bands, which plays an important role in the noise performance or sensitivity of the multi-band, multi-standard receiver. The values of capacitors *Cex1* and *Cex2* have to be determined the matching conditions for upper band and lower band. For the output impedance matching, *SW1* and *SW2* decide the load at the output. The on and off positions of these switches will set the output impedance matching of the LNA either to operate at upper band or lower band mode.

REFERENCES

[1] Adiseno, Håkan Magnusson and Håkan Olsson “ *A 1.8-V Wide-Band CMOS LNA for Multiband Multistandard Front-End Receiver*”

[2] Mohd Tafir Mustaffa, Aladin Zayegh, Ronny, Tun Zainal Azni Zulkifli, “*0.18 µm Fully Integrated 900 MHz CMOS LNA with Input and Output On-chip matching for Multi-standard Mobile Receiver*”,2008 International conference on Microelectronics.

[3] Aly Ismail and Asad A. Abidi, “*A 3–10-GHz Low-Noise Amplifier With Wideband LC-Ladder Matching Network*”. IEEE Journal Of Solid-State Circuits, Vol. 39, No. 12, December 2004.

[4] Pietro Andreani, Henrik Sjöland, *“Noise Optimization of an Inductively Degenerated CMOS Low Noise Amplifier*”. IEEE Transactions On Circuits And Systems—Ii: Analog And Digital Signal Processing, Vol. 48, No. 9, September 2001.

[5] Adiseno, Håkan Magnusson and Håkan Olsson “ *A 1.8-V Wide-Band CMOS LNA for Multiband Multistandard Front-End Receiver*”

[6] Shinde Jitendrakumar Namdeo and Dr S. K. Bodhe “A 1GHz to 3GHz Design of Low Noise Amplifier for Multi-Standard Receiver” *IJEST Vol.5, No.4 April 2013, Pp 665-676.*

AUTHOR'S PROFILE

Shinde Jitendrakumar N.

was born on June 25th 1975.He received his BE degree in the field of Electronics and Telecommunications Engineering in 1997 from Shivaji University, Kolhapur. He has completed ME in Electronics Engineering at GCOEP, affiliated to University of Pune in 2009. His research interests are in Wireless Communication He has 16 yrs of teaching experience. He has published Six Paper in International Journal and three papers in International and National Conferences.

Dr. S. K. Bodhe

born in Pune, India on Sept. 16th 1959. He received bachelor‟s degree in E & TC in 1983, M.E. in 1987 and Ph. D. in 1997 from Shivaji University, Kolhapur. He started his career as a R&D engineer turned teacher after 3 years. He became Assistant Professor in 1990 in Walchand College of Engineering in Sangli and Professor in 1999 in Pune Institute of Computer Technology. Currently he is working as a Principal, College of Engineering, Pandharpur, India. His area of interest is wireless networks.

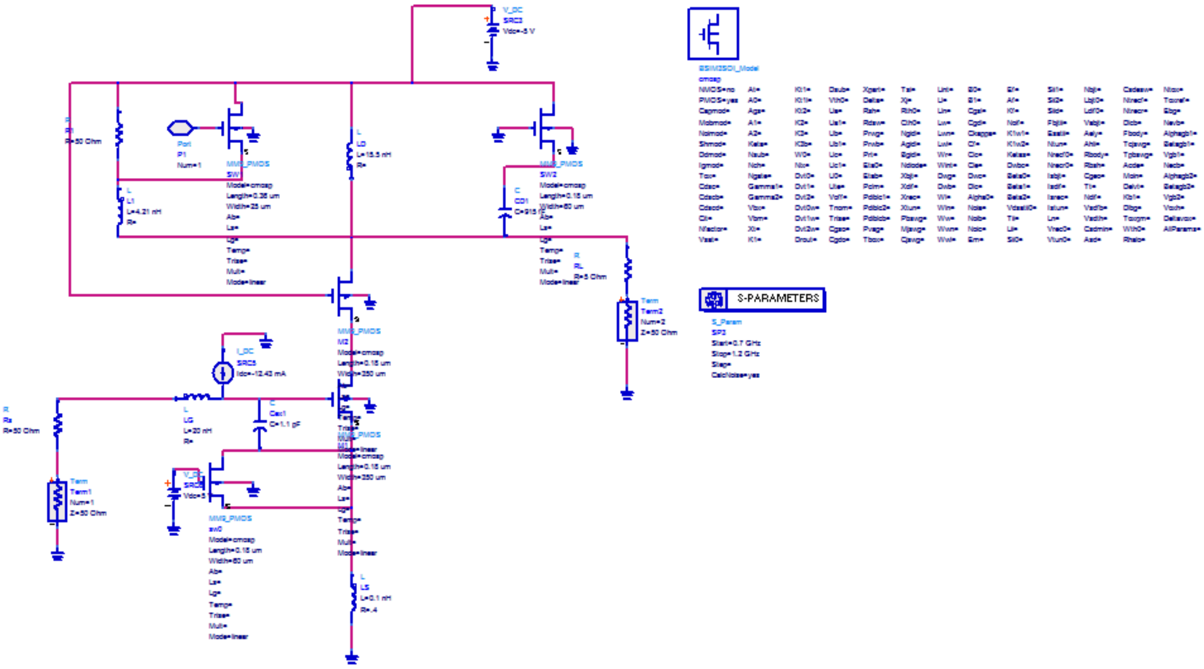


Fig.19. Low Noise Amplifier For Lower Band

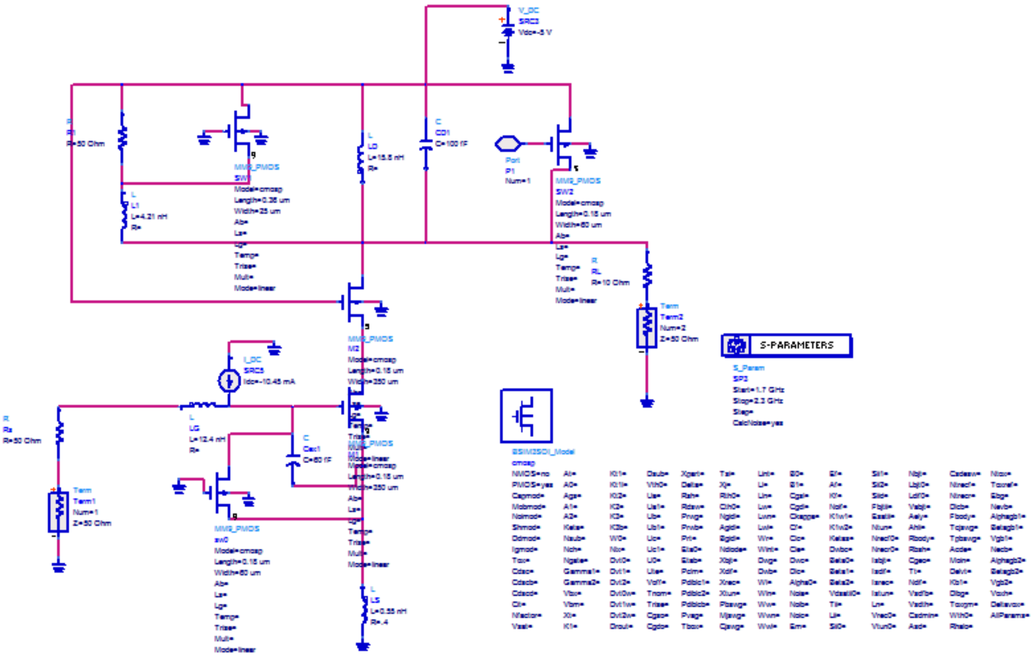


Fig.20. Low Noise Amplifier For Upper Band