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Low-Power Maximum a Posteriori (MAP) Algorithm for WiMAX Convolutional Turbo Decoder

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Abstract **- We propose to design a Low-Power Memory-Reduced Traceback MAP iterative decoding of convolutional turbo code (CTC) which has large data access with large memories consumption and verify the functionality by using simulation tool. The traceback maximum a posteriori algorithm (MAP) decoding provides the best performance in terms of bit error rate (BER) and reduce the power consumption of the state metric cache (SMC) without losing the correction performance. The computation and accessing of different metrics reduce the size of the SMC with no requires complicated reversion checker, path selection, and reversion flag cache. Radix-2*2 and radix-4 traceback structures provide a tradeoff between power consumption and operating frequency for double-binary (DB) MAP decoding. These two traceback structures achieve an around 25% power reduction of the SMC, and around 12% power reduction of the DB MAP decoders for WiMAX standard.**

Keywords- **Low-Power Design, Maximum a Posteriori (MAP) Algorithm, Turbo Decoder.**

I. INTRODUCTION

Turbo codes were presented in 1993, by Berrou et al and since then these codes have received a lot of interest from the research community as they offer better performance than any of the other codes at very low signal to noise ratio.Turbo codes achieve near Shannon limit error correction performance with relatively simple component codes. Turbo codes have shown their outstanding performance in terms of bit error rate (BER) at very low signal-noise ratio (SNR) since they appeared in the early 1990s.For this reason, they have been adopted in various standards for wireless communication systems such as DVB-RCS and IEEE 802.16.When the turbo codes were introduced by Berrou et.al in 1993,their decoding complexity was very high for them to be efficiently implemented in hardware when compared with a decoder for convolutional codes like a Viterbi decoder. Two-step Soft output Viterbi algorithm (SOVA) decoder offers a low complexity solution to the turbo decoder [2].However; the SOVA turbo decoder has less BER performance than the MAP turbo decoder for the same SNR. The MAP algorithm provides the best performance in BER while its complexity is higher than the two-step SOVA. This algorithm determines the probability of whether each received data symbol is a '1' as well as a'0'.This is done with the help of the data, parity symbols and the decoder knowledge of the encoder trellis. A trellis is a form of a state transition table, of the encoder input/output. Based on the data and parity information, the MAP decoder omputes the probability of the encoder being in a particular state.

Depending on the soft data, parity value and the weight from the previous state, the probability that the data is a can be computed. The MAP decoder computes the weight for each data symbol in a given block for both the forward and reverse directions. This results in the computation of forward and reverse metrics. The single binary (SB) CTC has been adopted in the forward-error-control (FEC) scheme for wideband code-division multiple access (WCDMA) and CDMA 2000. In 1999, the non-binary CTC was introduced, which has superior coding performance as compared with the SB-CTC. In recent years, double-binary (DB) CTC has been adopted in the FEC coding of advanced wireless communication standards.

The Turbo decoder attempts to reconstruct transmitted values through a series of decoding steps. Decoding strategy is based on the exchange of information between SISO (Soft Input Soft Output) component decoders in an iterative fashion [10]. The iterative turbo decoder structure is shown in Fig 1. Decoding is split in two steps in correspondence with the two encoding stages.

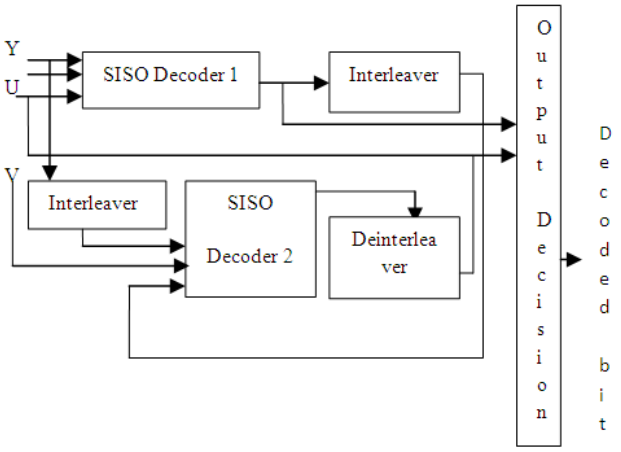

Fig.1 Iterative Turbo Decoder Structure

The interleaver permutes the data bit to support the error correction algorithm. The output from one decoder is fed into the other decoder through an interleaver/deinterleaver to help the later decoder make a better decoding decision in subsequent decoding iterations. Multiple iterations are required before the decoder converges to a final result [3]. After a pre specified number of decoding iterations, the final decision is made in the decision block by combining the outputs from both decoders [26]. The most widely used soft-values at the output of decoder are log-likelihood ratios-L_R (LLR's) [2].A decoder-binary circular turbo decoder is based on border metric encoding. With the proposed method, the memory size for branch memory is

reduced by half and the dummy calculation is removed at the cost of the small sized memory which holds the encoded border metrics. An energy-efficient SISO decoder based on the border metric encoding is suitable for the non-binary circular turbo codes [25].The proposed SISO decoder can reduce the energy consumption compared to the SISO decoder based on the dummy calculation and table-based interleaver.

II. Overall Block Diagram

The architecture can be divided into the forward recursion path (upper path) and backward recursion path (lower path). One branch metrics unit (BMU) for (1a),one NRP for (1b) or (1c),one SMC with depth L/2,one proposed TRP, one LAPO for (1d),ne log-extrinsic module (LEX) for (1e),and one hard decision module (HD) for (2) are used for each path. When the TRPs are removed, the PE performs the conventional-type EML-MAP decoding. The branch metrics are directly calculated without buffering in a branch metrics cache because of the D-type decoding method [1].The proposed traceback MAP decoding is to reduce the power consumption of the SMC. The traceback MAP decoding has five major stages/phases:

B. Branch Metrics

The branch metrics are computed with the received codeword and the a priori LLR in the natural order by using the hamming distance. However, instead of Hamming distance, Euclidean distance may be used to calculate the branch metric. If the demodulated symbols are directly decoded as single bits they are treated as "hard" symbols. In other words, if the demodulated symbols are quantized to 3or 4 bit values, they are treated as "soft" symbols [1].

B. Natural Recursion Professor (NRP)

The forward (or backward) state metrics are recursively computed by the NRP with the branch metrics in the natural order. In the trackback decoding procedure, the six difference metrics are computed by the NRP [4].

C. State Metrics Cache (SMC)

SMC stores the forward (or backward) recursion state metrics to compute the a posteriori LLP until the backward (or forward) recursion state metrics are generated [5]. Note that the difference metric is the difference between two state metrics and has the same bit-length of the state metric.

D. Trackback Recursion Processor (TRP)

The forward (or backward) state metrics are recursively traced back by the TRP with the stored difference metrics in the reverse order. Concurrently, the backward (or forward) state metrics are recursively computed with the branch metrics [10]. The TRP, composed of two TBUs, traces the eight state metrics back with the stored six difference metrics. The two TBUs, radix-2*2 traceback structure has low hardware costs, and the radix-4 traceback structure has short path delays.

E. Log-A Posteriori Module (LAPO)

The a posteriori LLP is composed with regenerated forward (or backward) state metric, the backward (or forward) state metrics, and branch metrics by the LAPO in the reverse order. The extrinsic values and hard bits are computed in the reverse order with the a posteriori LLP [10].

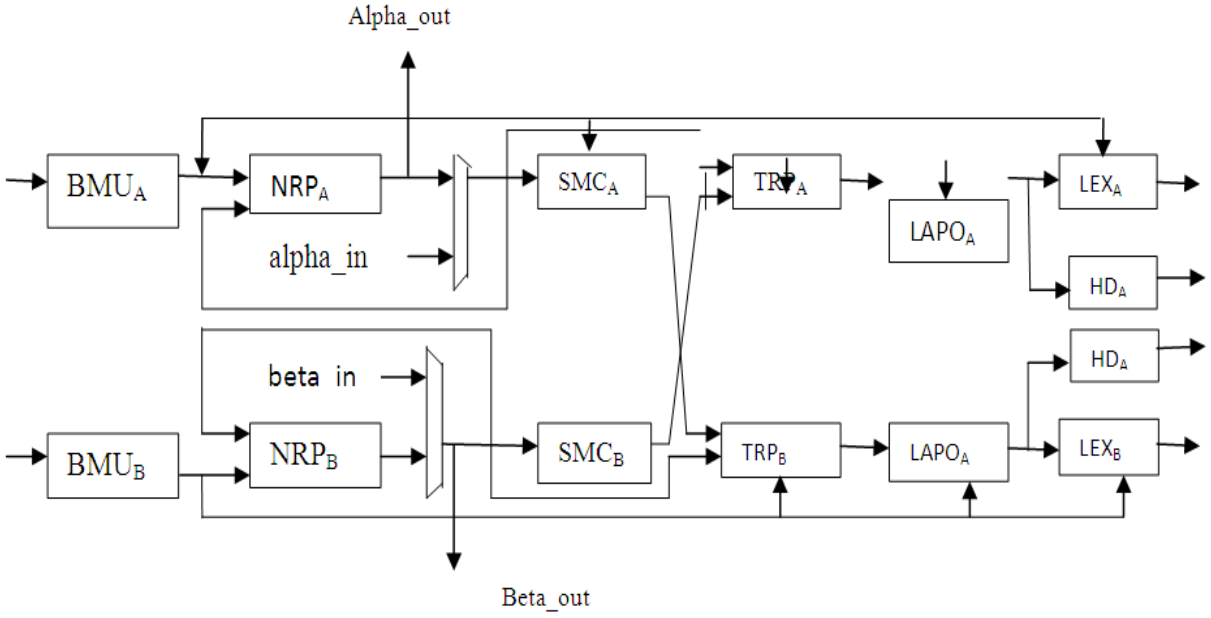

Fig.2. Block diagram of Traceback MAP decoder

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III. State Metric Cache (SMC)

The proposed memory-reduced traceback MAP decoding is the background information of SMC power reduction for the MAP decoder. It follows two decoding procedure; they are

- Conventional decoding procedure.
- Reverse decoding procedure.

A. Conventional Decoding Procedure

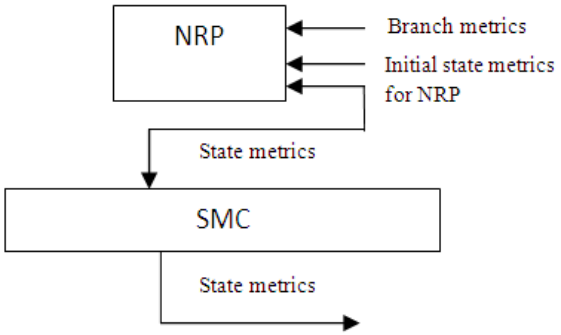

Fig.3. Conventional Decoding Procedure

Despite the SB or DB MAP decoding, forward and backward recursion states metrics are computed in chronologically reverse order. Both forward and backward recursion state metrics are required for the computation of a posteriori LLP [4]. Thus, a large SMC stores the forward (or backward) recursion state metrics to compute the a posteriori LLP until the backward (or forward) recursion state metrics are generated. In the natural order, the NRP, composed of add-compare-select units (ACSUs), is used to recursively compute the forward (or backward) recursion state metric in cycles [17]. The obtained state metrics in cache cycle are immediately stored into the SMC and recursively fed back to the NRP to calculate the next state metrics [6]. To compute the a posteriori LLR, the state metrics are read out from the SMC. The SMC of the conventional decoding procedure still accounts for more than 50% of the entire power consumption [8].

B. Reverse Decoding Procedure

To further reduce the access power of SMC, the reverse computations modified the conventional decoding procedure for the radix-2 SB MAP decoding. The decoding procedure of the reverse computations is illustrated in Fig. 4. Compared with the conventional decoding procedure shown in Fig. 3, the reverse decoding procedure adds a reversion checker, a reversion flag cache, and a reverse recursion processor (RRP).

The reversion checker decides whether the state metrics computed by the NRP are reversible or not. If a state metric is not reversible, this state metric is stored in one sub bank of the SMC. Meanwhile, the reversion flag cache stores the path information of this state metric. To compute a posteriori LLP, the irreversible state metric is read out from the SMC according to the path information stored in the reversion flag cache. Otherwise, the reversible state metric is computed by the RRP, composed of reverse units [20].

The recovered state metrics are recursively fed back to the RRP to calculate the next reversible state metrics. The reverse computations reduce the power consumption of the radix-2 SB MAP decoder, because the sub banks of SMC are dynamically accessed, and the computational power of the reversion checker and RRP is small [7]. The reverse computations for the radix-2 SB L-MAP decoding achieve an around 30% power reduction with over 20% logic overhead [9]. In addition, dividing the SMC into sub banks increases the silicon area of the SMC and consumes more overall power of the SMC if all sub banks are accessed [1].

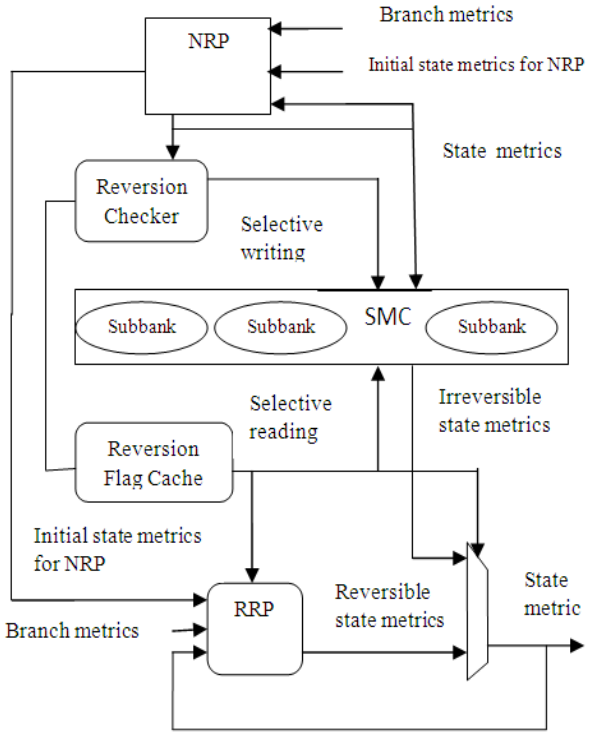

Fig.4. Reverse Decoding Procedure

IV. Traceback Recursive Processor

The proposed traceback computation requires no complicated reversion checker, path selection and reversion flag cache. In the traceback path unit, the difference metrics computed by the NRP are stored in the SMC[15]. Then, the state metrics are traceback with the stored difference metrics by the traceback recursion processor (TRP) in the reverse order. The power consumption of the SMC can be reduced by accessing the difference metrics because the number of stored metric is lower. The computational power of TRP is small, and the overall memory size and power consumption of the traceback path is reduced. The TRP, composed of 2 TBU's, traces the eight state metrics back with the stored six difference metrics. Compared with the conventional decoding procedure, the stored metrics are reduced from eight state metrics to six difference metrics [18]. Thus, the traceback computation reduces the SMC power consumption for the DB MAP decoding. For the traceback DB MAP decoding, two traceback structures are

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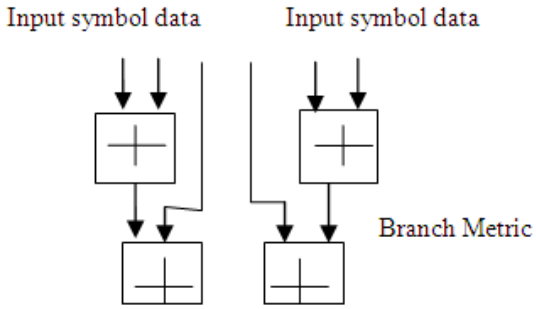
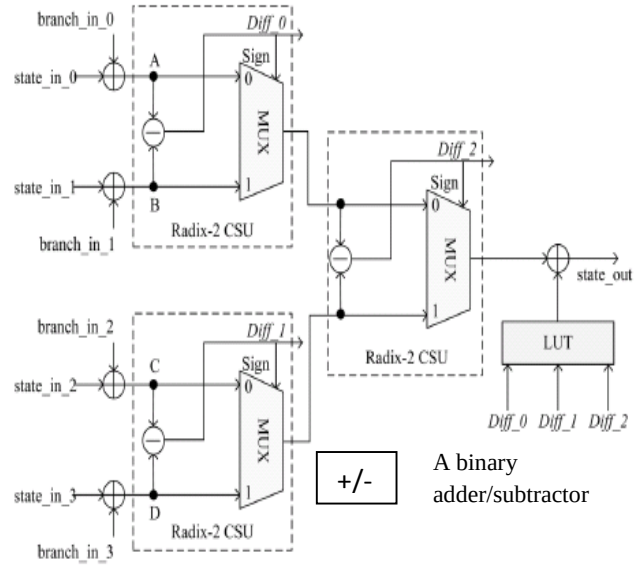
demonstrated. The radix-2*2 traceback structure has low hardware costs, and the radix-4 traceback structure has short path delays.

Branch Metric Unit



A. Radix-2x2 Traceback pair

For the radix-4 MAP decoding two types of ACSU's, the radix-2*2 ACSU and the radix-4 ACSU are widely used to constitute the NRP, Fig. 5 shows an example of the radix-2*2 ACSU. The radix-2*2 ACSU consists of four front adders, three radix-2 compare-select units (CSUs), and an LUT.



Diff_0=A-B
Diff_1=A-B
Diff_2=MAX (A,B)-MAX (C,D)

Fig.5. Add-Compare Select Unit of Radix-2*2 Traceback pair

In the proposed traceback computation, three difference metrics (Diff 0, Diff 1, Diff 2) generated by three radix-2*2 CSU's are stored in the SMC. Fig. 6 shows corresponding TBU of the radix-2*2 ACSU. Fig. 5 illustrates a computational example of the radix-2*2 ACSU and TBU. The radix-2*2 ACSU obtains the maximal state metric B based on Diff 0, Diff 1 and Diff 2. Subsequently, the radix-2*2 TBU regenerates A, B, C and D based on Diff 0, Diff 1 and Diff 2, since B can be initially achieved. Hence, the four state metrics can be recomputed by the radix-2*2 TBU with the difference metrics stored in the SMC. In the radix-2*2 TBU, the sign bit of the difference metric decides the path of the multiplexers and the operation of the binary/subtracted. The storage of the SMC is reduced from eight state metrics to six difference metrics at cache stage. Note that the values A, B, C and D in the output end of the radix-2*2 TBU can be the input values of the LAPO to compute. This approach reduces eight addresses in the LAPO [1].

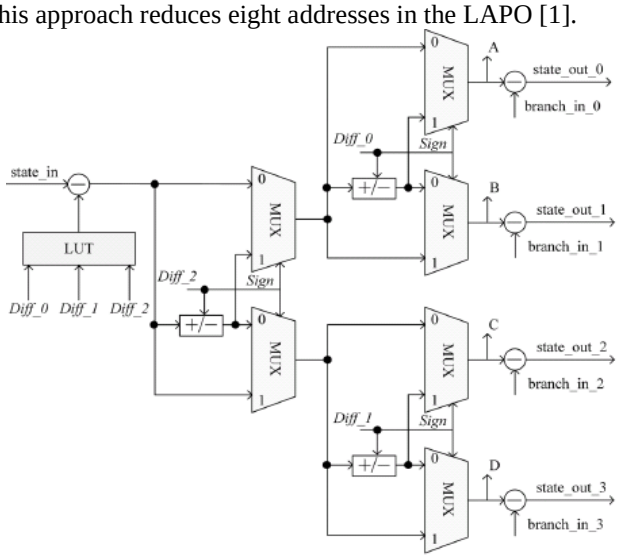
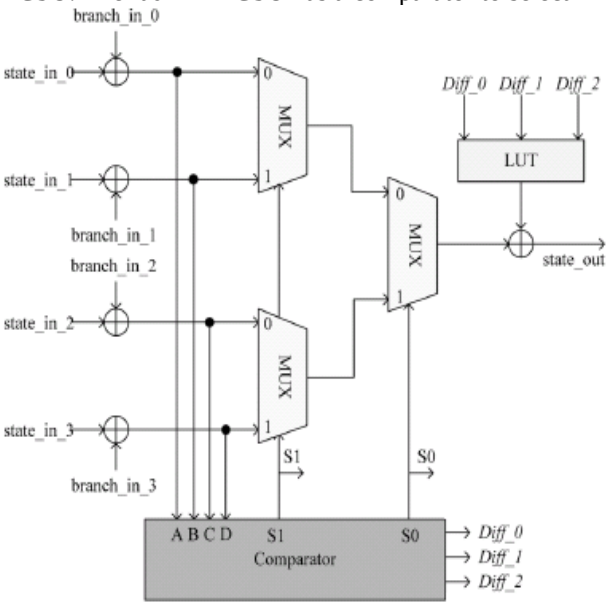


Fig.6. Traceback unit Radix-2*2 Traceback pair

B. Radix-4 Traceback Pair

For the radix-4 MAP decoding, two types of ACSUs,the radix-2*2 ACSU and the radix-4 ACSU are widely used to constitute the NRP, Fig. 7 shows an example of the radix-4 ACSU. The radix-4 ACSU has a comparator to select



Diff_0=A-B
Diff_1=A-C
Diff_2=A-D

Fig.7. Add-Compare Select Unit of Radix-4 Traceback pair.

maximal state metric quickly. Unlike the radix-2*2 ACSU, three difference metrics related to A (Diff 0,Diff 1,and Diff 2) and two selective bits (S0 and S1) of the radix-4 ACSU obtains the maximal state metric B based on two

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selective bits generated by the six parallel subtraction in the comparator. The three difference metrics related to A are stored in the SMC [13]. Since B can be initially achieved, A can be regenerated by the radix-4 TBU based on the stored S0 and SI. Subsequently, the radix-4 TBU regenerates A, B, C and D based on Diff 0, Diff 1 and Diff 2.The storage of the SMC is reduced from eight state metrics to six differences metrics and four extra bits at each stage [6].The values A,B,C and D in the output end of the radix-4 TBU can be the input values of the LAPO to compute. This approach reduces eight adders in the LAPO.The proposed traceback computation and traceback pair of the radix-4 DB MAP decoding can be simply applied to the radix-4 SB MAP decoding with a simple trellis modification [1].

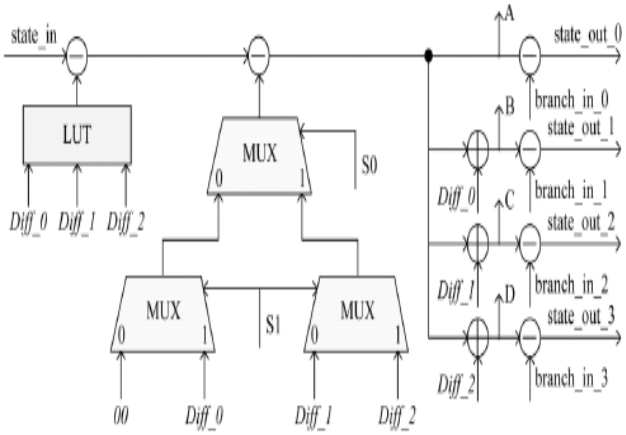

Fig.8. Traceback unit Radix-4 Traceback pair

V. Result and Discussion

The power consumption of SMC is reduced by the traceback MAP decoding with a low logic for codeword received by the branch metric unit. The radix-2*2 ACSU has the longest path delay, because the values of the latter radix-2 CSU in the radix-2*2 ACSU are not correct until the sign (most significant) bits of the two former radix-2 ACSU are stable as shown in Fig.9. The radix-2*2 TBU does not suffer from this problem because the sign bits of the difference metrics are initially known. However, the radix-2*2 traceback structure has less area costs and power consumption as shown in Fig.10. Compared with the radix-2*2 traceback structure, the radix-4 traceback structure has shorter and more balanced path delays. The radix-4 ACSU has a comparator to select the maximal state metric quickly as shown in Fig.11.The generated output end of the radix-4 TBU can be the input values of the LAPO to compute in as shown in Fig.12. The power consumption and memory size of state metric cache are reduced by using two traceback structures, radix-2*2 and radix-4.

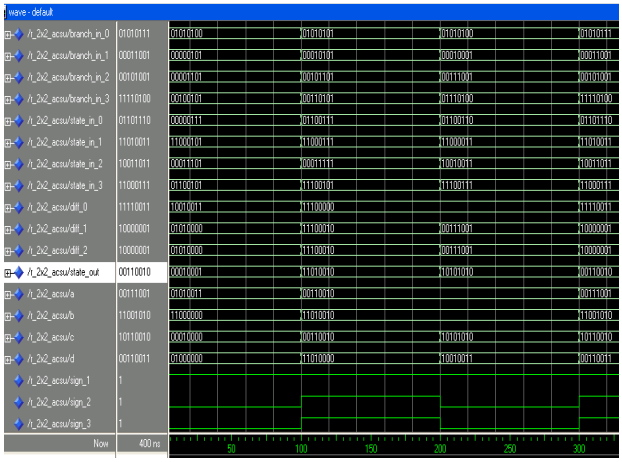

Fig.9 Radix-2*2 add-compare selects unit waveform

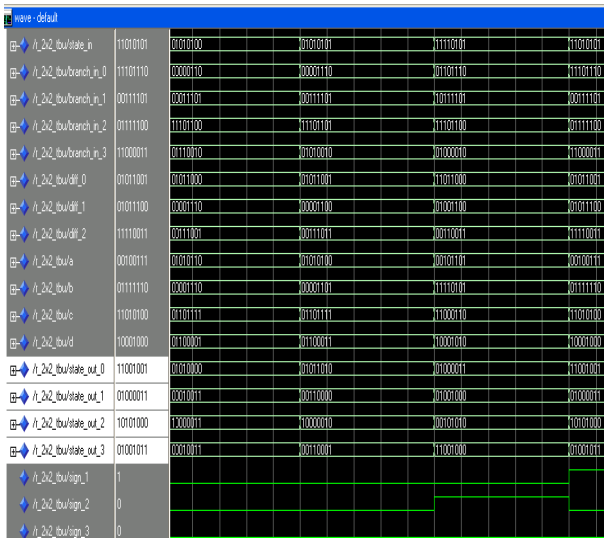

Fig. 10 Simulation result for Traceback unit of Radix-2*2 Traceback pair.

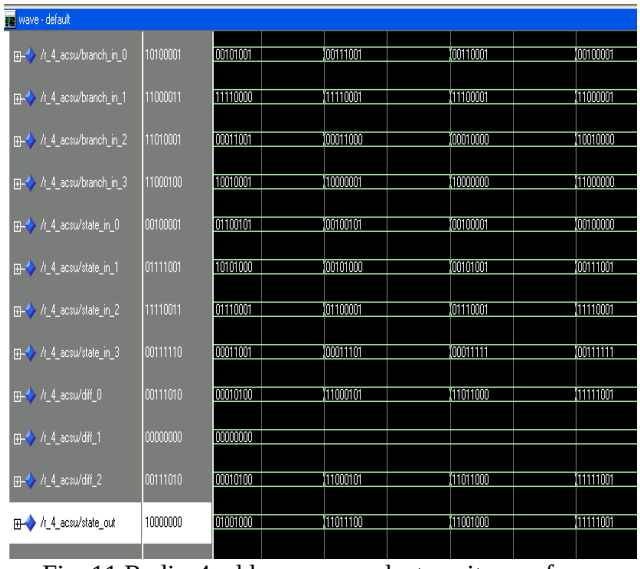

Fig. 11 Radix-4 add-compare selects unit waveform

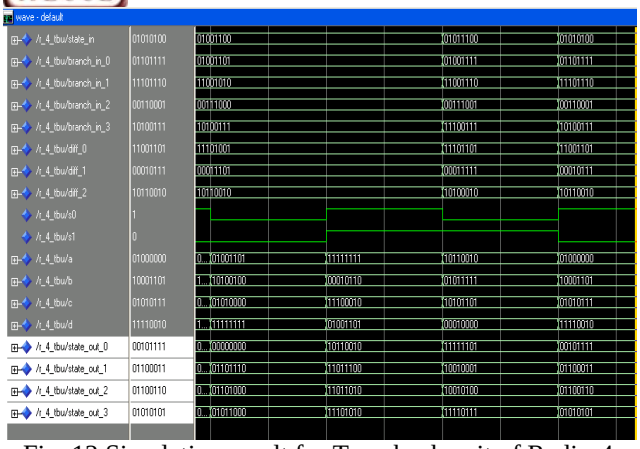

Fig. 12 Simulation result for Traceback unit of Radix-4 Traceback pair

Table 1: Comparison table for radix-2*2 and radix-4 Traceback structure

Calculated value	Radix-2*2	Radix-4
Power	38 (mw)	50 (mw)
Gate count for design	35,469	36,399

VI. CONCLUSIONS

The traceback MAP decoding performed in the L-MAP and (E) ML-MAP without losing correction ability. The traceback radix-2*2 pair has low hardware costs. The experimental result shows that the traceback structure achieves an around 25% power reduction of the SMC, and around 12% power reduction of ten DB MAP decoders for the WiMAX CTC. The traceback of MAP decoding algorithm reduces power consumption and reduced memory sized. Employing the proposed reverse calculation scheme reduces the state memory size by 50%. Therefore, the total memory size is reduced by 39.2%. The size of branch memory is reduced by half and the dummy calculation that is complex in non binary turbo codes is completely removed at the cost of a small memory that holds encoded border metrics.

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