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Simulation of Nine Level Cascaded H-bridge Multilevel DC-Link Inverter

N. Booma, Nagisetty Sridhar

***Abstract* – This paper presents simulation of the nine level cascaded H-bridge multilevel inverter based on a multilevel DC link (MLDCL) and a bridge inverter to reduce the number of switches. An MLDCL can be a diode-clamped phase leg, a flying-capacitor phase leg, or cascaded half-bridge cells with each cell having its own DC source. Compared to diode clamped & flying capacitor type MLDCL inverters cascaded H-bridge multilevel inverter requires least no of components to achieve same no of voltage levels. Optimized circuit layout is possible because each level have same structure and there is no extra clamping diodes or capacitors. Soft switching techniques can also be used to reduce switching losses and device stresses. The MLDCL provides a DC voltage with the shape of a staircase approximating the rectified shape of a commanded sinusoidal wave to the bridge inverter, which in turn alternates the polarity to produce an AC voltage. Compared with the existing type of cascaded H-bridge multilevel inverter, the MLDCL inverters can significantly reduce the switch count as well as the number of gate drivers as the number of voltage levels increases. For a given number of voltage levels, the required number of active switches is 2 (m-1) for the existing multilevel inverters, but it is m+3 for the MLDCL inverters. This paper aims to present analysis and simulation of cascaded H bridge multilevel dc link inverter. Matlab simulation has been done and simulation results of the cascaded H-bridge MLDCL inverter supplying induction motor load is discussed and it is proved that proposed inverter output has less THD compared to flying capacitor and diode clamped multilevel inverter.**

***Keywords* — Cascaded half bridge, multilevel dc link, multilevel inverter, reduced component count, switching sequences.**

I. INTRODUCTION

The voltage source inverters produce an output voltage or current with levels either 0 or $\pm V_{dc}$. They are known as the two-level inverter. To produce a quality output voltage or a current wave form with less amount of ripple content, they require high switching frequency. In high- power and high-voltage applications these two level inverters, however, have some limitations in operating at high frequency mainly due to switching losses and constraints of device ratings [1]. These limitations can be overcome using multilevel inverters. The multilevel inverters have drawn tremendous interest in power industry. It may be easier to produce a high-power, high-voltage inverter with multi level structure because of the way in which the voltage stresses are controlled in the structure[3].

The unique structure of multilevel voltage source inverters allows them to reach high voltages with low harmonics without use of transformers or series connected synchronized-switching devices. As the number of voltage levels increases, the harmonic content of the output voltage wave form decreases significantly. There are 3 types of multilevel inverters named as diode clamped multilevel inverter, flying capacitor multilevel inverter and cascaded multilevel inverter. These three types of multilevel inverters requires more no of components such as switches, clamping diodes and capacitors[10]. As the number of voltage levels m grows the number of active switches increases according to 2×(m-1) for the cascaded H-bridge multilevel inverters.

This paper presents a nine level cascaded H-bridge multilevel inverter based on an MLDCL and a bridge inverter. Compared with the existing cascaded multilevel inverters, the cascaded MLDCL inverters can significantly reduce the switch count as well as the number of gate drivers as the number of voltage levels increases. For a given number of voltage levels m, the cascaded MLDCL inverter requires m+3 active switches, roughly half the number of switches Simulation results are included to verify the operating principle of the proposed MLDCL inverters.

II. CASCADED H-BRIDGE MLDCL INVERTER TOPOLOGY

Figure.1 shows a block diagram of the presented cascaded H-bridge MLDCL inverter topology, which consists of a multilevel DC source to produce DC-link bus voltage V_{bus} and a single-phase full-bridge (SPFB) inverter consists of four switches S1-S4 to alternate polarity of DC-link bus voltage to produce an AC voltage. The DC source is formed by connecting a number of half-bridge cells in series with each cell having a voltage source controlled by two switches S_{ak} and S_{bk}. The two switches and operate in a toggle fashion. The cell source is bypassed with S_{ak} on and S_{bk} off, or adds to the dc-link voltage by reversing the switches. Figure.2 shows a circuit diagram of the presented cascaded H-bridge MLDCL inverter topology.

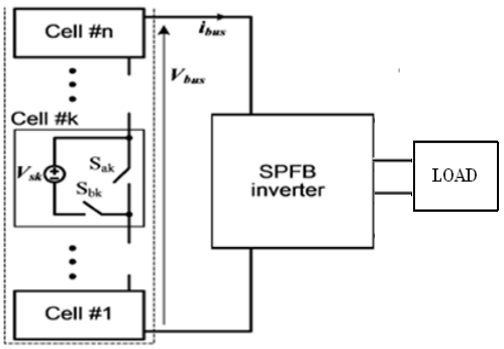

Fig.1. Block diagram of Cascaded H-bridge MLDCL inverter

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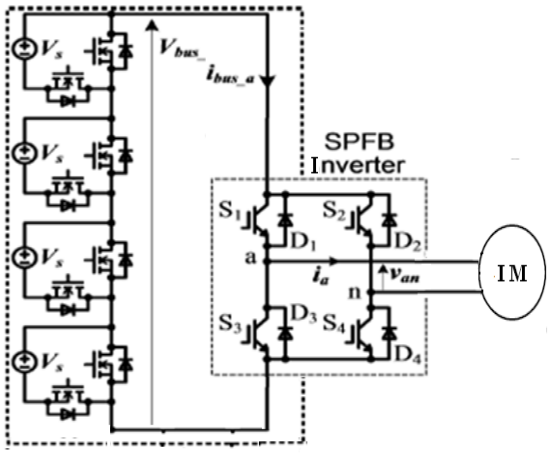

Fig.2. Circuit diagram of Cascaded H-bridge MLDCL inverter

The circuit diagram of the cascaded H-bridge multilevel DC-link inverter topology shown in Figure 2 consists of multilevel DC-link voltage source and single phase full bridge inverter.

A. Multilevel DC-link voltage source

Multilevel DC-link *voltage* source is formed by connecting a number of half-bridge cells in series with each cell having a voltage source controlled by two MOSFET switches as shown in the Figure 3. The two MOSFET switches will operate in a toggle fashion. Low on resistance and fast switching capability, low voltage MOSFETS are utilized in each cell source to reduce the inverter cost or to provide a high bandwidth sinusoidal output voltage. The MOSFET switches are triggered by proper switching signals to produce multi level DC-link bus voltage which is indicated by V_{bus} in the circuit diagram.

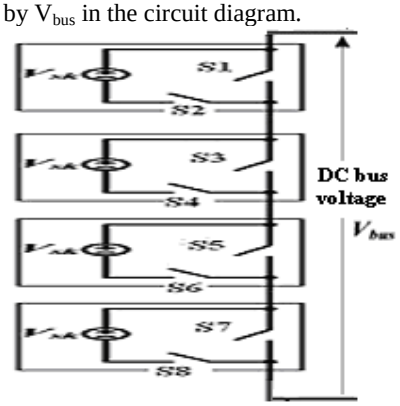

Fig.3. Multilevel DC-link voltage source

Various modes of switching sequence is given in the table 1 to produce DC bus voltage V_{bus} with the shape of stair case with (n=4) steps, where n is the number of cell sources that is given to the SPFB inverter.

Based on the various modes given in table 1 switching signals are generated for the switches in the half bridge cells. The switching pulses are shown in Figure 4.

Table 1: Various modes of switching sequence to produce DC bus voltage

	SWITCH STATE							
SW NO / MODE	S1	S2	S3	S4	S5	S6	S7	S8
0 I	1	0	1	0	1	0	1	0
0.001 II	0	1	1	0	1	0	1	0
0.002 III	0	1	0	1	1	0	1	0
0.003 IV	0	1	0	1	0	1	1	0
0.004 V	0	1	0	1	0	1	0	1
0.006 VI	0	1	0	1	0	1	1	0
0.007 VII	0	1	0	1	1	0	1	0
0.008 VIII	0	1	1	0	1	0	1	0
0.009 IX	1	0	1	0	1	0	1	0
0.01	1 - ON 0 - OFF							

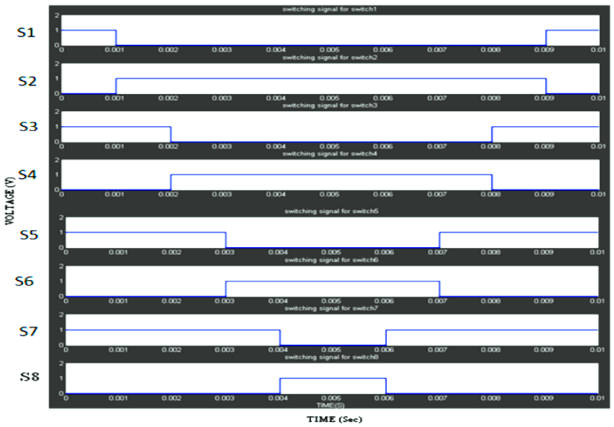

Fig.4. Switching pulses for switches in four H-bridge cells

By giving the switching pulses shown in figure 4 to the switches in four H-bridge cells the MLDCL voltage source produces DC bus voltage V_{bus} with the shape of stair case with (n=4) steps that approximates the rectified waveform of the commanded sinusoidal voltage, where n is the number of cell sources that is given to the SPFB inverter.The desired DC bus voltage V_{bus} is shown in the Figure 5.The switches in four cells will operate at twice of the fundamental frequency of the output voltage.

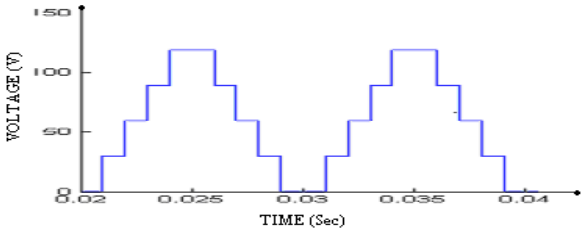

Fig.5. Desired DC bus voltage Vbus of cascaded H-bridge MLDCLI

B. Single phase full bridge inverter

The single phase full bridge (SPFB) inverter shown in Figure 6(a) consists of four IGBT switches S1-S4 which can switch at faster rates and have less demanding gate drive requirements compared to the GTOs in two level inverters.

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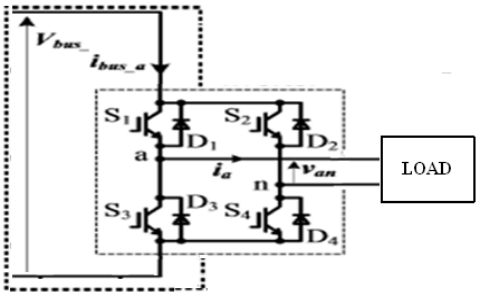

Fig.6(a) Block diagram of SPFB inverter

The switches S1-S4 always work in pairs such that S1&S4 triggered for positive half cycle and S2&S3 will trigger with some delay to produce negative half cycle by operating the switches at the fundamental frequency of the output voltage. The switching sequence for producing multilevel AC output voltage is shown in Figure 6(a).

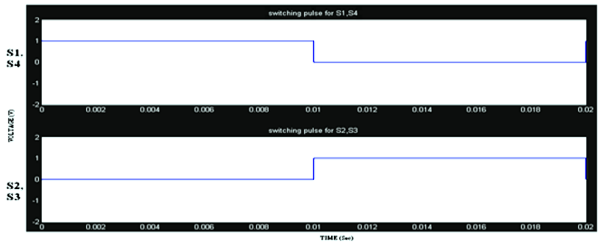

Fig.6(b) Switching signals of SPFB inverter

C. Principle of operation of nine level cascaded H-bridge MLDCL inverter

The principle of operation of nine level cascaded multilevel DC-link inverter is explained by explaining the operating principles of multilevel DC link voltage source and single phase full bridge inverter. To produce nine level AC output voltage V_{an} the multilevel DC-link source is formed by connecting four H-bridge cells in series with each cell having a separate voltage source controlled by two switches S_{ak} and S_{bk} which will operate in a toggle fashion. The cell source is bypassed with S_{ak} on and S_{bk} off, or adds to the DC link bus voltage by reversing the switches. The DC bus voltage V_{bus} is fed to the SPFB inverter.

The switching signals shown in Figure 6(b) are given to the SPFB inverter in turn to alternate the voltage polarity of the DC bus voltage V_{bus} for producing an AC output voltage V_{an} of a stair case shape with (2n+1)=9 levels, whose voltages are $-(V_1+V_2+.....+V_n)$, $-(V_1+V_2+.....V_{n-1})$.....,$-V_2$, $-V_1$,0, V_1, V_2,.....$(V_1+V_2+....V_{n-1})$, $(V_1+V_2+....V_n)$. Where V_1, V_2.....V_n are voltages of cell sources. The desired AC output voltage $V_{an\ of}$ cascaded H-bridge is shown in the Figure 6(c).

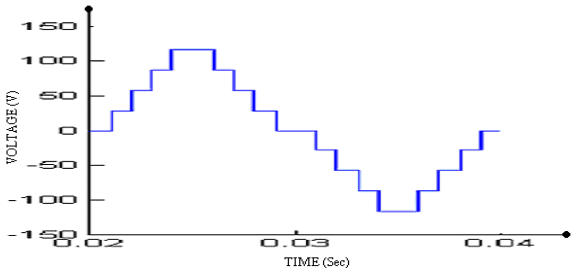

Fig.6(c) Desired AC output voltage Van of cascaded H-bridge MLDCLI

III. SIMULATION RESULTS

A detailed circuit simulation was conducted to verify the operating principles of the proposed MLDCL inverters.

A. Nine level cascaded H-Bridge MLDCL Inverter with R load

A single-phase 9-level cascaded H-bridge MLDCL inverter was first studied for powering a resistive load, as shown in Figure 7. The load resistance is 30Ω and the voltage of each DC source is set at 30 V for an output frequency of 50 Hz.

The DC bus voltage $V_{bus,}$ AC output voltage of the inverter V_{an} and AC output current i_{an} are shown in Figures 7(a), 7(b) and 7(c) respectively. These waveforms confirm the principle of operation of 9-level cascaded H-bridge MLDCL inverter described in section II-C.

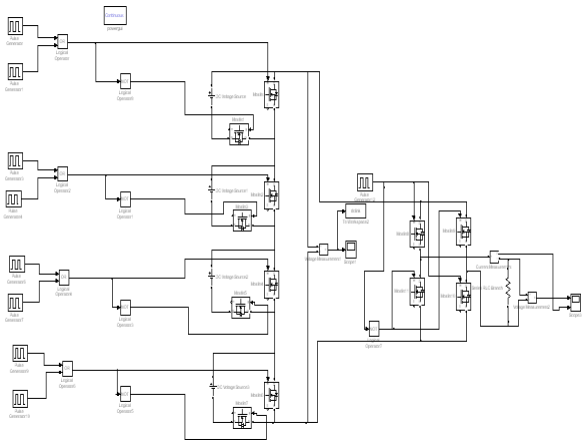

Fig.7. Simulation circuit of nine level cascaded H-Bridge MLDCL Inverter with resistive load

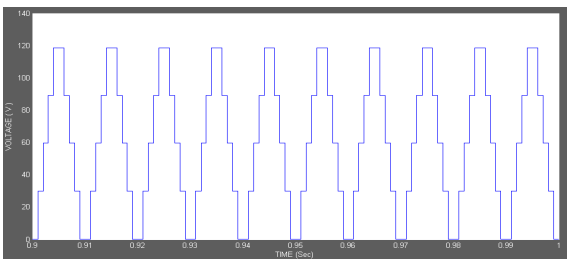

Fig.7 (a) Simulated DC bus voltage waveform of nine level cascaded H-Bridge MLDCL Inverter with resistive load

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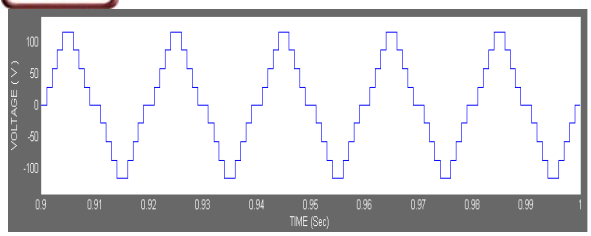

Fig.7 (b) Simulated AC output voltage waveform of nine level cascaded H-Bridge MLDCL Inverter with resistive load

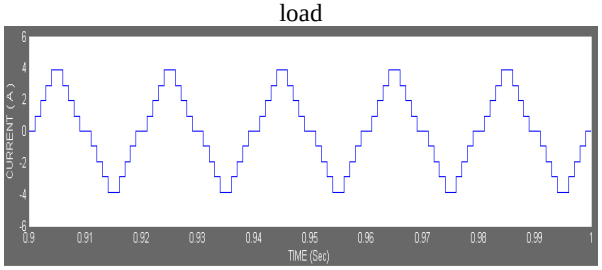

Fig.7 (c) Simulated AC output current waveform of nine level cascaded H-Bridge MLDCL Inverter with resistive load

B. Nine level cascaded H-Bridge MLDCL Inverter with RL load

A single-phase 9-level cascaded H-bridge MLDCL inverter was studied for powering an inductive resistor load, as shown in Figure 8. The load resistance and inductance are 30Ω and 90 mH and 150 mH. The voltage of each DC source is set at 25 V for an output frequency of 50Hz.

The simulated DC bus voltage $V_{bus,}$ AC output voltage of the inverter V_{an} and AC output current i_{an} are shown in Figures 8(a), 8(b) and 8(c) respectively. These waveforms confirm the principle of operation of 9-level cascaded H-bridge MLDCL inverter described in section II-C with an inductive resistor load.

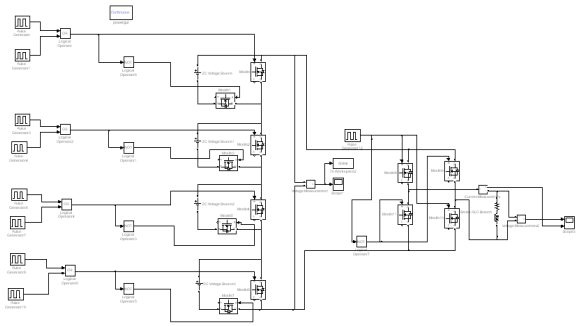

Fig.8. Simulation circuit of nine level cascaded H-Bridge MLDCL Inverter with inductive resistor load

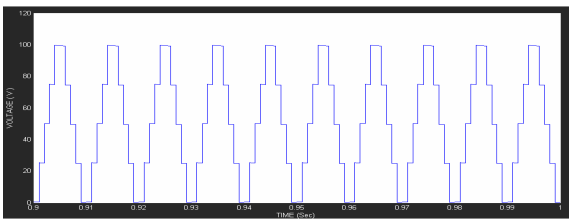

Fig.8 (a) Simulated DC bus voltage waveform of nine level cascaded H-Bridge MLDCL Inverter with inductive resistor load

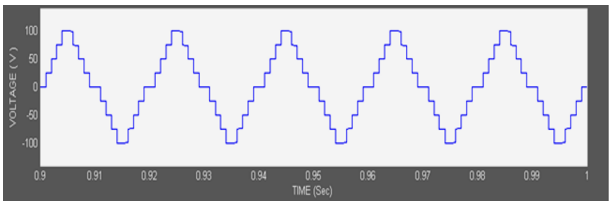

Fig. 8 (b) Simulated AC output voltage waveform of nine level cascaded H-Bridge MLDCL Inverter with inductive resistor load

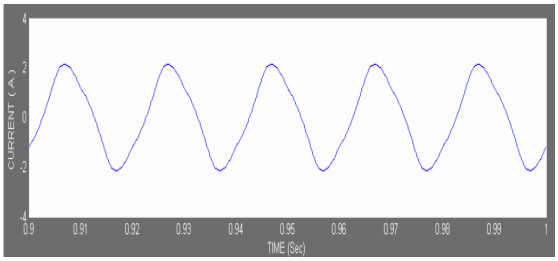

Fig.8(c) Simulated AC output current waveform of nine level cascaded H-Bridge MLDCL Inverter with inductive resistor load

The output voltage and current are in phase with each other for resistive load but there exists a phase lag between output voltage and current for an inductive resistor load due to presence of inductance in the load. The phase lag increases with the increase in inductance value. The simulated AC output current waveform with increased load inductance is shown in Figure 8(d).

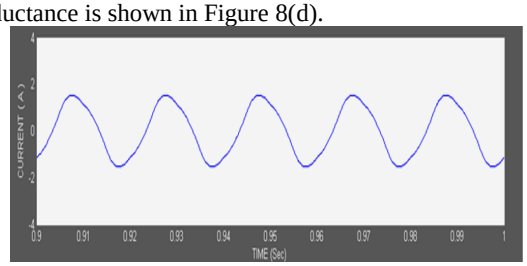

Fig.8(d) Simulated AC output current waveform of nine level cascaded H-Bridge MLDCL Inverter with inductive resistor load with increased load inductance.

The line spectrum for the output current waveform is taken to determine the Total Harmonic Distortion present in the waveform. The Figure 9 shows the Total Harmonic Distortion is 7.24% for the output current of nine level cascaded H-Bridge MLDCL Inverter with RL load with increased load inductance.

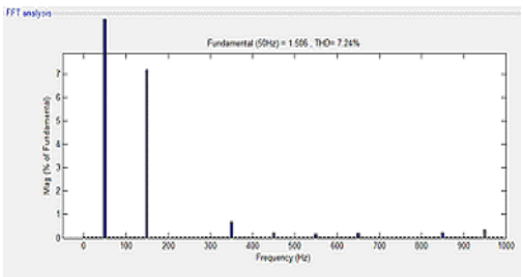

Fig.9. FFT analysis of output current waveform of nine level cascaded H-Bridge MLDCL Inverter with inductive resistor load

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C. Nine level cascaded H-Bridge MLDCL Inverter with induction motor load

A single-phase 9-level cascaded H-bridge MLDCL inverter was studied for powering an induction motor load, as shown in Figure 10. The rating of the motor are power 1HP, voltage 230V. Main winding resistance and inductance are 2.02 Ω and 0.0074 H and auxiliary winding resistance and inductance are7.14 Ω and 0.0085 H. The voltage of each DC source is set at 80 V to get 220 V rms voltage required for motor to run for an output frequency of 50 Hz.

The simulated AC output voltage of the inverter V_{an} and AC output current i_{an} are shown in Figures 10(a)and 10(b) respectively. These waveforms confirm the principle of operation of 9-level cascaded H-bridge MLDCL inverter described in section II-C with an induction motor load.

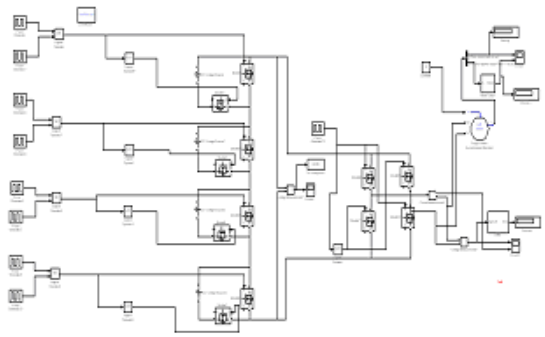

Fig.10. Simulation circuit of nine level cascaded H-Bridge MLDCL Inverter with induction motor load

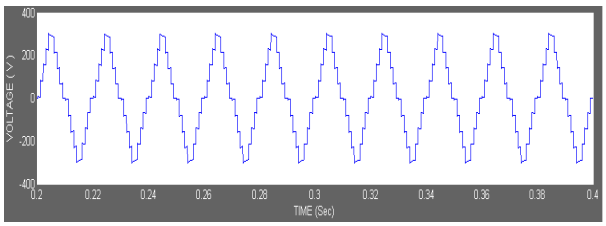

Fig.10. (b) Simulated AC output voltage waveform of nine level cascaded H-Bridge MLDCL Inverter with induction motor load

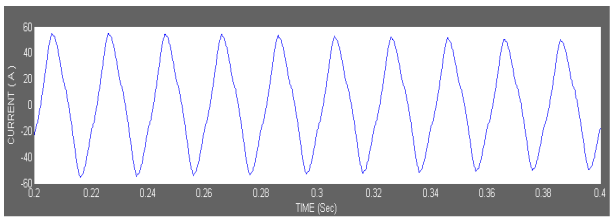

Fig.10. (c) Simulated AC output current waveform of nine level cascaded H-Bridge MLDCL Inverter with induction motor load.

The line spectrum for the output current waveform is taken to determine the Total Harmonic Distortion present in the waveform. The Figure 11 shows the Total Harmonic Distortion is 10.77% for the output current of nine level cascaded H-Bridge MLDCL Inverter with induction motor load.

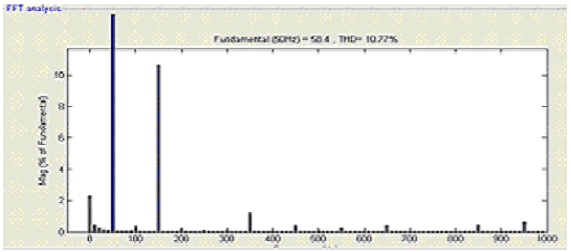

Fig.11. FFT analysis of output current waveform of nine level cascaded H-Bridge MLDCL Inverter with induction motor load

D. Comparison of the nine level cascade MLDCL Inverter and the existing MLI

From the previous discussions, it is demonstrated that the MLDCL inverters can significantly reduce the component count. Fig. 12 plots a chart for comparison of the required number of switches between the proposed MLDCL inverter and the cascaded H-bridge counterpart. As the number of voltage levels m grows, the number of active switches required is 2*(m-1) =16 for existing cascaded multilevel inverter and m+3 =12 switches are required for cascaded H-bridge MLDCL inverter[8]

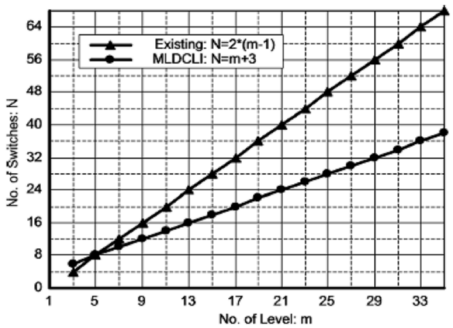

Fig.12. Comparison of required number of switches.

IV. CONCLUSION

The presented nine level cascaded H-bridge MLDCL inverters can eliminate roughly half the number of switches, their gate drivers compared with the existing cascaded MLI counterparts. Despite a higher total VA rating of the switches, the cascaded MLDCL inverters are cost less due to the savings from the eliminated gate drivers and from fewer assembly steps because of the substantially reduced number of components, which also leads to a smaller size and volume.

One application area in the low-power range (≤ 100 kW) for the MLDCL inverters is in permanent-magnet (PM) motor drives employing a PM motor of very low inductance.The MLDCL inverter can utilize the fast-switching low-cost low-voltage MOSFETs in the half-bridge cells, and the IGBT's in the single-phase bridges to dramatically reduce current and torque ripples and to improve motor efficiency by reducing the associated copper and iron losses resulting from the current ripple. These configurations may also be applied in distributed power generation involving fuel cells and photovoltaic cells.

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