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Characterization of Resistive Dividing Comparator in Deep Sub-Micron Region

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Abstract — **In this paper Resistive Dividing comparator along with the Buffer stage in 130nm and 90nm technologies is presented. The supply voltage V_{DD} for this comparator is 1.3v and 1v for 130nm and 90nm respectively. Various analysis of different characteristics of the comparator has been carried out such as offset, ICMR, propagation delay, speed, power dissipation in both the technologies and the result has been compared for both the technologies. The speed of the comparator as measured from the simulation results is 1.06GHz and 1.23 GHz along with the power dissipation of 167mV and 71mV for 130nm and 90nm CMOS process respectively.**

Keywords — **Buffer stage, latch comparator, resistive dividing network.**

I. INTRODUCTION

A comparator is a circuit which compares one analog signal with the other analog signal or reference signal and gives a binary output depending on the comparison. The function of the comparator is to decide that which of two applied inputs has larger value. The most useful application of the comparator is in converting an analog signal into digital signal. The comparator is also considered as 1- bit ADC. While designing the comparators the factors which are to be considered are Propagation delay, Offset voltage, Input common mode range, Power dissipation.CMOS dynamic latched comparators are very useful for varied applications such as high-speed analog-to-digital converters (ADCs), memory sense amplifiers (SAs) and data receivers due to fast-speed, low-power consumption, high-input impedance and full-swing output. The positive feedback mechanism is used by CMOS dynamic latch comparators. By using dynamic latched comparators instead of using pre-amplification stage [1] [2] much of the silicon area can be reduced. By replacing traditional amplifier chain based comparators they are helpful in achieving low power consumption. In this paper the focus has been made on resistive dividing comparator.

II. RESISTIVE DIVIDING COMPARATOR AND BUFFER STAGE

A. Resistive Dividing Comparator

Fig.1. shows the schematic of resistive dividing comparator. The circuit is in reset mode when the Clk signal goes low. As The Clk is low nMOS transistor M9 is off and hence circuit will get disconnected from the V_{SS}. At the same time, pMOS transistors M13 and M6 are on and hence the outputs will be precharged upto VDD.

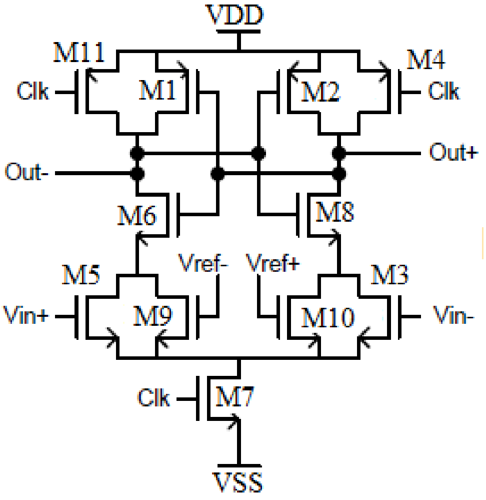

Fig.1. Resistive Dividing comparator[1]

The circuit works in regenerative mode when the Clk signal goes high. As the Clk is high the nMOS transistor M9 are on and the pMOS transistors M6 and M13 will be off. In regenerative mode the circuit compares the input voltages with the help of transistors which will be operated in triode region.

B. Buffer Stage

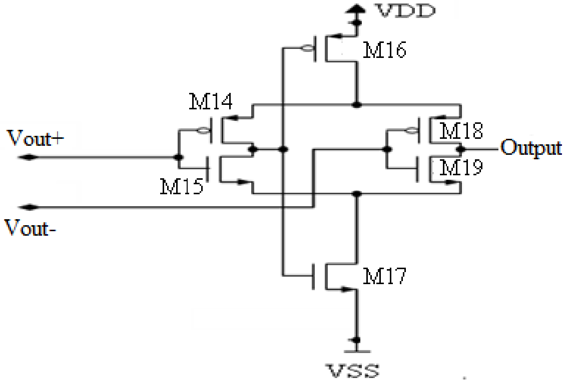

Fig. 2. Output Buffer circuit [5].

The output buffer circuit used in the comparator is shown in fig.2[5]. The output buffer stage is also known as post amplifier. This circuit is self biasing differential amplifier which has differential inputs as Vout+ & Vout- and does not have any slew rate limitations. It is also useful in giving the output in proper shape.

III. DESIGN METHODOLOGY

Fig.3 shows the circuit diagram of comparator consisting of resistive dividing network and output buffer stage. The two ended output of the resistive dividing comparator are Vout+ & Vout-. Both the outputs of the comparator are inputs to the buffer. Thus the two ended output of resistive dividing comparator is being converted into single ended output for different types of analysis.

Table I : CMOS Transistor widths and lengths for different Technologies

Technology	Wp(um)	Wn(um)
130nm	0.15	0.15
90nm	0.12	0.12

Table I given above shows different widths of the transistor to be used according to the chosen technology. The length for the transistor is 0.13um and 0.1um respectively for 130nm and 90nm technology.

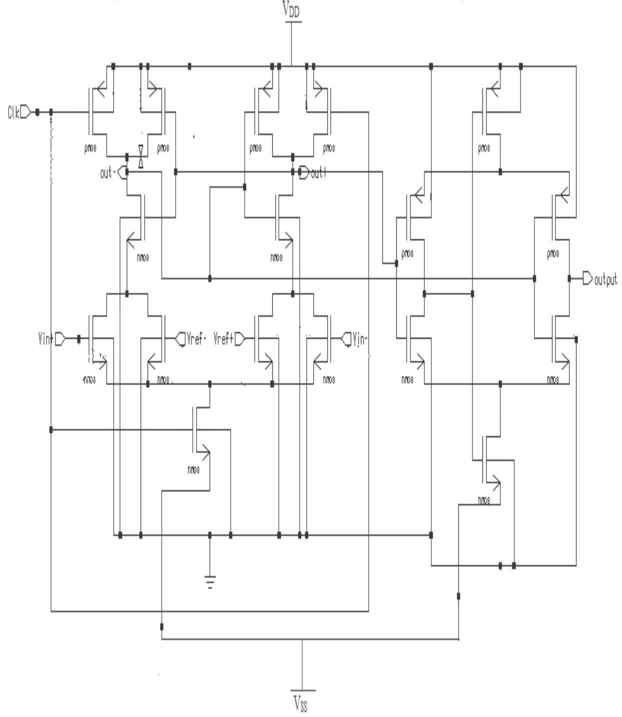

Fig.3. Design of comparator

IV. SIMULATED RESULTS OF THE COMPARATOR

The simulated results are obtained for two different technologies 130nm and 90nm. In table II, different voltage values are given for supply voltage VDD and VSS, reference voltage Vref+ and Vref-, input voltage Vin+ and Vin-.

Table II : Different voltage values for different Technologies

Voltage Terminals(v)	Technology	
	130nm	90nm
Vdd	1.3	1
Vss	-1.3	-1
Clk	1.3	1
Vin+	1.3	1
Vin-	1.3	1
Vref+	0.26	0.45
Vref-	-0.26	-0.45

A. Simulated Waveforms in 130nm

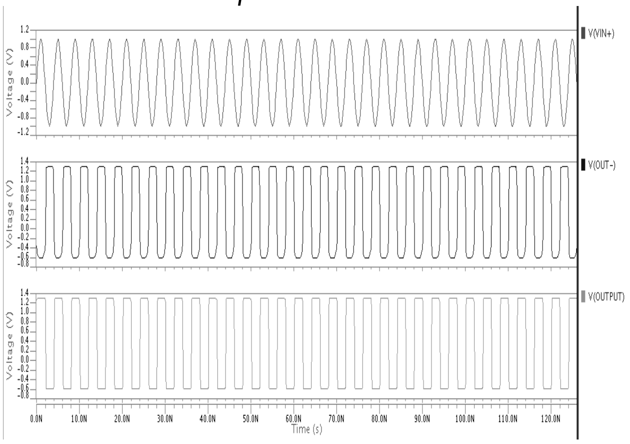

Fig.4. Input as sine wave.

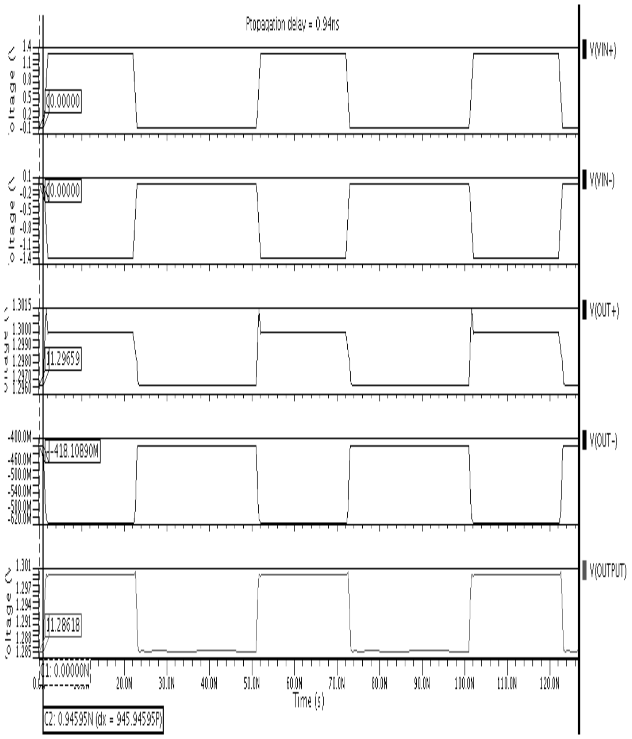

Fig.5. Transient response.

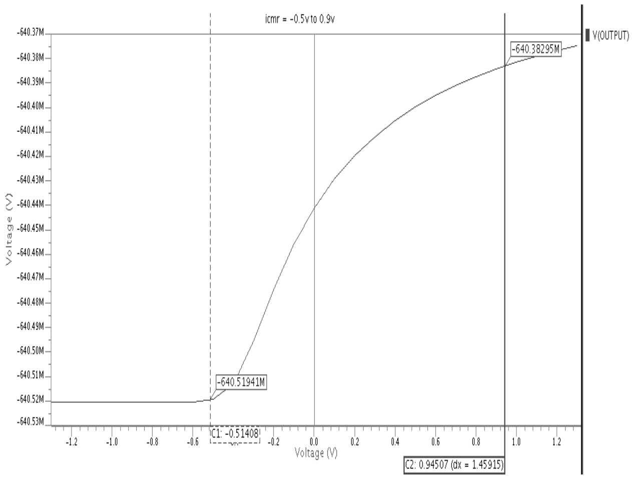

Fig.6. Input Common Mode Range.

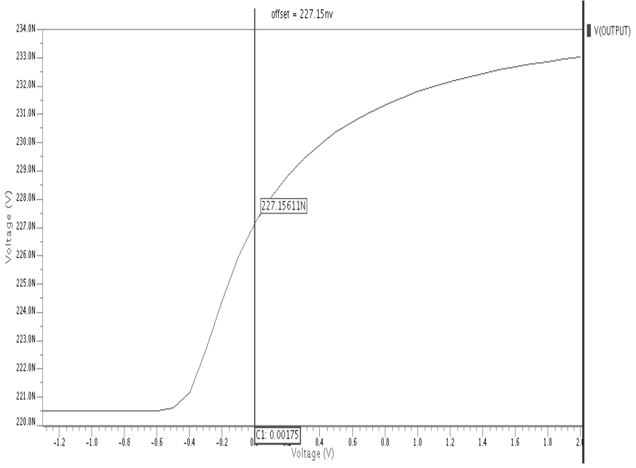

Fig.7. Offset voltage

B. Simulated Waveforms in 90nm

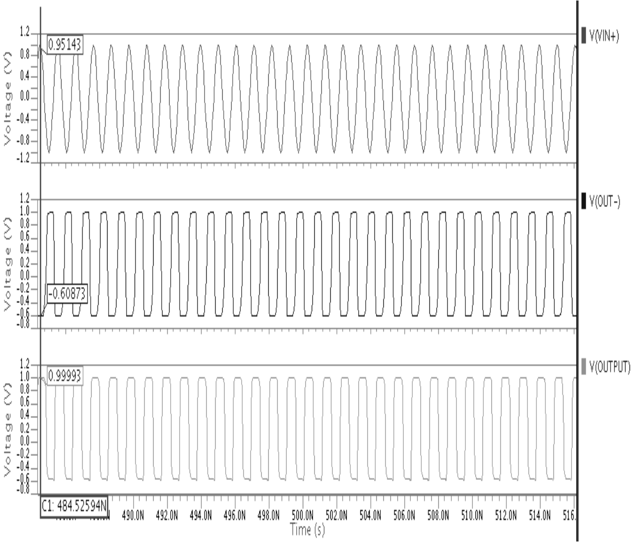

Fig.8. Input as sine wave.

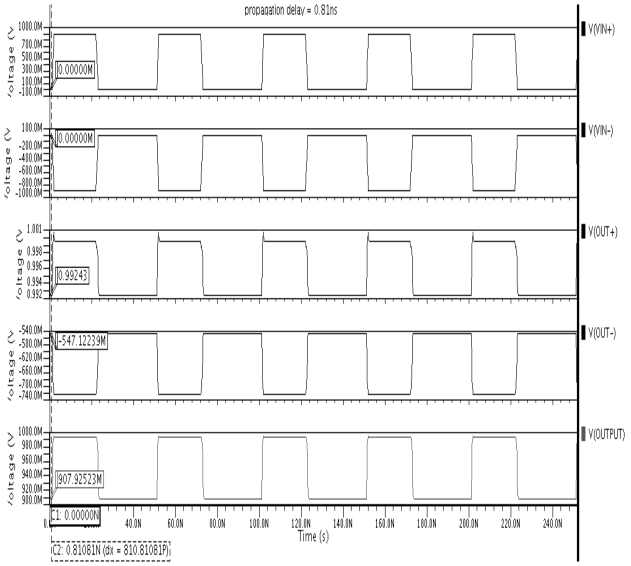

Fig.9. Transient response.

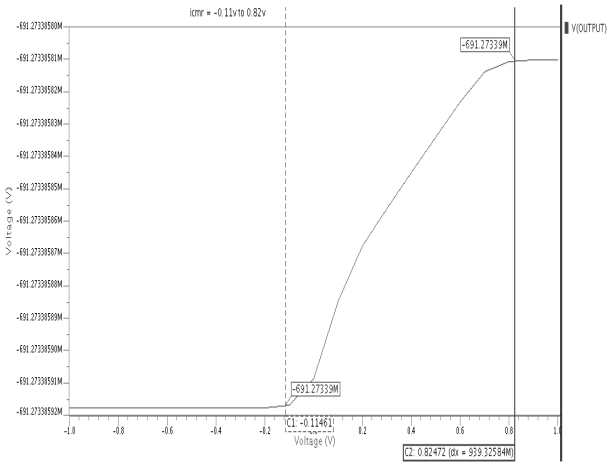

Fig.10. Input Common Mode Range

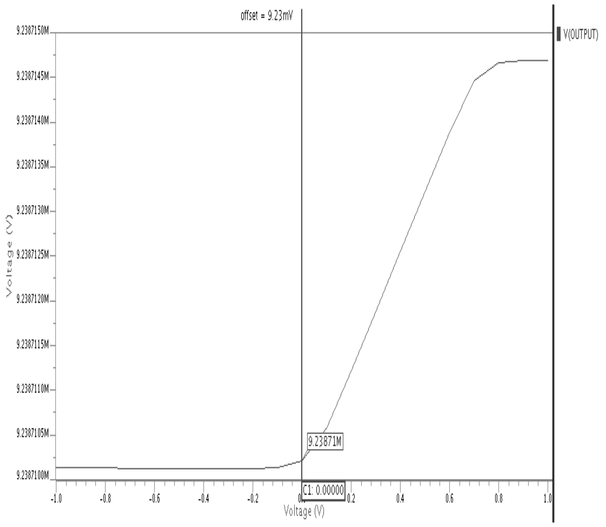

Fig.11. Offset Voltage [6]

V. CONCLUSION

In this paper, simulated results are presented for the comparator for two different technologies, 130nm and 90nm. The summary of the comparison for the comparator in both the technologies is given in the table III.

Table III : Different measured parameter values for different Technologies

Parameters	Technology	
	130nm	90nm
Propagation Delay (ns)	0.94	0.81
Speed(GHz)	1.06	1.23
ICMR(V)	-0.5 to 0.9	-0.11 to 0.82
Offset	227.15nV	9.23mv
Power Dissipation(mV)	167	71

From the table shown above it can be concluded that as the technology scales down the propagation delay is also decreased as a result of which speed of the comparator will increase. The input common mode range for the comparator in 130nm is higher as compared to 90nm. Because of the technology scaling, transistor non idealities increases and so is the offset voltage which also gets increased. The power dissipation is less in 130nm as compared to 90nm which means the power dissipation is reduced with the reduction in technology.

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