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2.79 GHz Low Phase Noise – Single Stage Source Coupled CMOS Voltage Controlled Oscillator (VCO) Using 0.18 µm CMOS Technolog

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***Abstract* — This paper present a single stage CMOS Voltage controlled oscillator with a high oscillation frequency and low power consumption. The VCO is a single stage circuit has a low phase noise due to reduced noise sources. The VCO is intended to operate as a frequency synthesizer in a PLL to generate local oscillator frequency (LO) for an acquisition system, providing in-phase/Q-phase outputs. The performance of the proposed circuit is evaluate in spice simulation by using Tanner software, the VCO we use S-Edit, T-Spice, W-Edit in a 0.18-µm standard CMOS process. The results show that the oscillation frequency of VCO may vary between 0.58 to -2.79 GHz. Also, the phase noise performance of the VCO at oscillation frequency of 2.79 GHz is better than other. For the 1.8v supply voltage, the power consumption is 0.72 mW at the same oscillation frequency.**

***Keywords* — Oscillators, phase-locked loop, low phase noise, voltage-controlled oscillator.**

I. Introduction

Transceivers for wireless communication system contain low-noise amplifiers, power amplifiers, mixers, digital signal processing chips, filters, and phase-locked loops. Voltage controlled oscillators play a critical role in communication systems, providing periodic signals required for timing in digital circuits and frequency translation in radio frequency Circuits. While oscillators exhibit periodically time-Varying Characteristics, this dissertation is concerned with an electrical signal at a specific Frequency. When it is used for frequency translation, we often refer to an oscillator as the Local oscillator (LO).A Typical PLL is made up of a VCO, low-pass loop filter, phase detector, and frequency divider. Because the PLL is involved in frequency translation and Channel selection, its spectral purity affects the performance of an overall wireless system. The spectral purity of the PLL output depends heavily on that of the VCO. Designing voltage controlled oscillators for this monolithic integration is always desirable but most challenging. The first requirement is to achieve high-frequency operation with reasonable power consumption. However, the most critical challenge for the VCO is the phase-noise performance. Finally, small chip area is important to monolithic system integration. In recent years, LC-tank oscillators have shown good phase-noise performance with low power consumption. However, there are some disadvantages. First, the tuning range of an LC-oscillator (around 10 _ 20%) is relatively low when compared to ring oscillators (>50%). So the output frequency may fall out of the desired range in the presence of process variation. Second, the phase-noise performance of the oscillators highly depends on the quality factor of on-chip spiral inductors. For most digital CMOS processes, it is difficult to obtain a quality factor of the inductor larger than three. Therefore, some extra processing steps may be required. Finally, on-chip spiral inductors occupy a lot of chip area, typically around 200 *200 -- 300 * 300 μm^2, which is undesirable for cost and yield consideration.

The ring oscillators, however, do not have the complication of the on-chip inductors required for the LC oscillators. In addition to a wide tuning range, ring oscillators with even number of delay cells can produce quadrature-phase outputs [1].The phase noise performance of ring oscillators is much poorer in general [1], [5]. Also, at high oscillation frequencies, the power consumption of the ring oscillators may not be low which is a key requirement for battery operated devices [7]. To overcome these problems, we work on single stage oscillator without an LC tank.

II. The Source Coupled CMOS Methodology

In a conventional ring oscillator designs, two or more delay elements are employed to satisfy the Barkhausen’s oscillation criteria. On the other hand, to enhance the oscillation frequency, the number of delay elements should be reduced. In the previous high oscillating frequency architectures, at least two delay cells are used to obtain a 180° phase shift [1], [8].The suggested oscillator enhances the oscillation frequency by reducing the number of the circuit stage to one. This feature also lowers the power consumption and improves the phase noise.

These circuits can be designed to dissipate less power than the ring oscillator and current-starved voltage controlled oscillator. The operation of the CMOS source coupled VCO in fig 1 is load MOSFETs M3 and M4 pull the output. The MOSFETs M5 and M6 behave as constant current source sinking a current Id. MOSFETs M1 and M2 act as switches. MOSFETM1 is off and M2 is on, because the voltage of terminal out2 is larger than voltage of terminal out1.Therefore current through MOSFET M2 is 2Id and the capacitor will be changed by current Id, because constant current source M6 sinking current Id.

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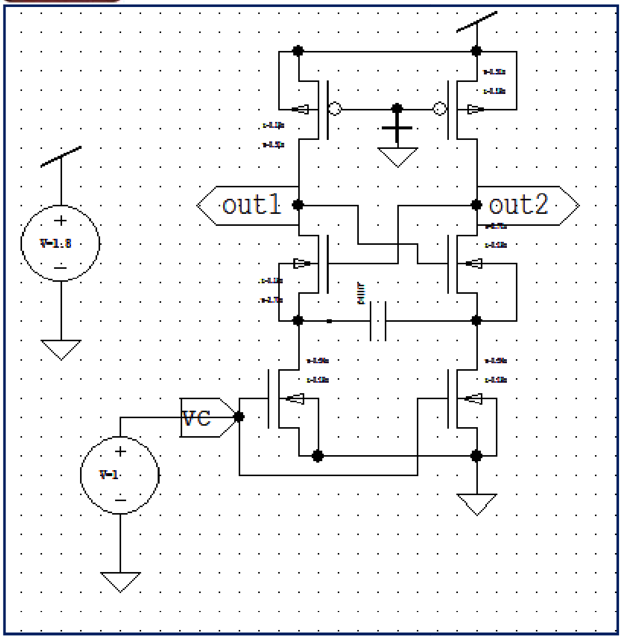

Fig.1. CMOS Source Coupled Voltage Oscillator

When the voltage of x and y capacitor terminal is same then capacitor is fully charged. The current Id through c, cause point x to discharge down towards ground.

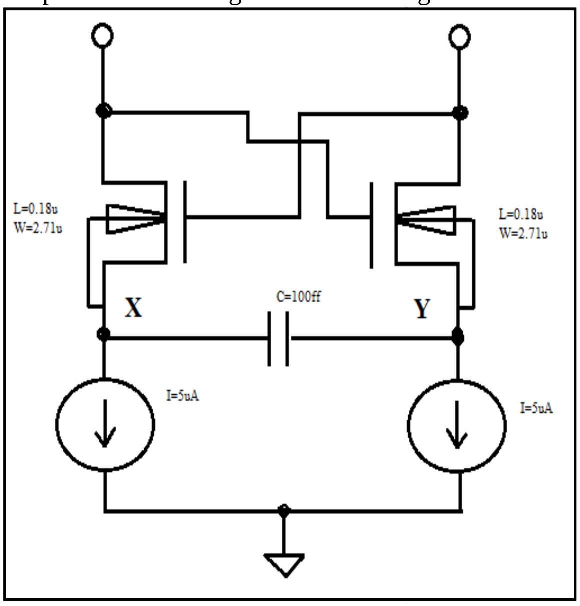

Fig.2. Schematic of CMOS Source Coupled Voltage Oscillator, M1 ON and M 2 is OFF.

When point x get down, M1 turn on and M2 turn off. The voltage of point X changed before switching took place the time it takes point X to change 2Vthn is given by,

$$\Delta t = c.\ 2.\ Vthn / Id. \quad (1)$$

Since the circuit is symmetrical two of these discharge time are needed for each cycle of oscillator the frequency of oscillation is given by,

$$Fosc = 1/2.\ \Delta t = Id / 4.c.\ Vthn \qquad (2)$$

III. Simulation Results

We performed spice simulation for proposed circuit by using Tanner software; we use S-Edit, T-Spice, W-Edit as a simulator. The result as compared in table II with other VCO. Source coupled VCO was simulated in a 0.18µm standard CMOS process with 1.8V as the power supply voltage. The central frequency of the VCO is about 2.79 GHz. The oscillation frequency of VCO versus the control voltage (Vc) is shown in table I. The out1 and out2 both are in 180° phase shift shown in Figure 3. The time domain behavior of VCO at 2.79 GHz frequency is also shown in Figure 4.The power consumption of VCO is 0.72mW as observed from the results. The proposed oscillator has lower power consumption while achieving a higher oscillation frequency. In addition, the proposed circuit has a large output voltage swing which helps to reduce the phase noise [5].

The oscillator is very compact due to the minimum stage number. Phase noise is defined as the difference between carrier power and noise power, phase noise performance can be improved reducing noise power. The phase noise performance is better than other circuits, especially considering its lower power consumption and higher oscillation frequency. This configurations useful When the VCO center frequency is set by external capacitor.

A. Oscillation Frequency

The following waveform shows that differential output out1 and out2 having Phase difference of 180^0.

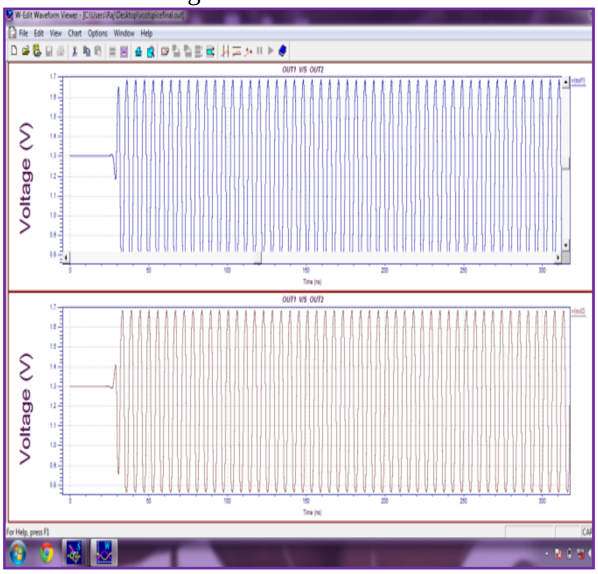

Fig.3. Out1 and out2 have a 180° phase shift

The following waveform is undamped oscillation of differential output voltage of out1 and out2.The following waveform shows an undamped oscillation of differential output voltage. The time domain of VCO at 2.79 GHz frequency is also shown in waveform.

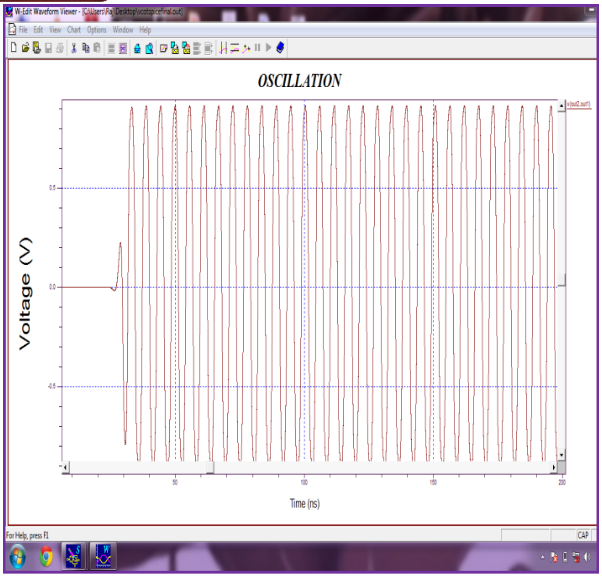

Fig.4. The output of VCO at 2.79 GHz

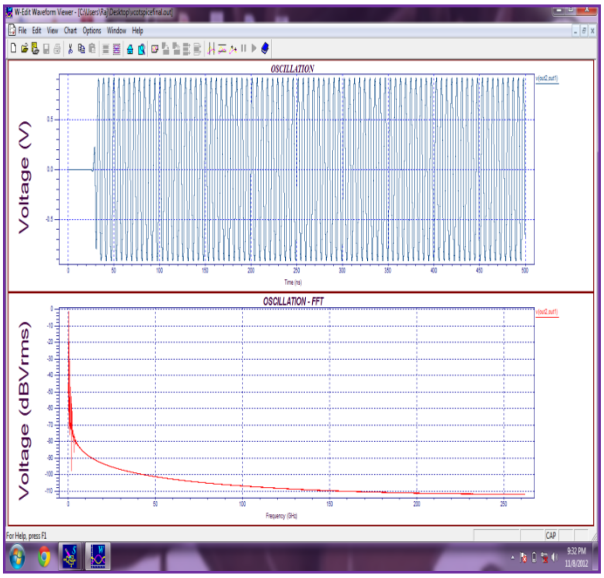

Fig.5. FFT of 2.79 GHz Oscillation

B. *Phase Noise*

Phase noise specification is very critical issue in designing of oscillator delay-cell. Before getting into design of delay-cell it is important to understand the phase noise limits for delay-cell based VCOs and how do they depend on delay-cell design parameters. There are mainly two types of approaches to deal with the phase noise of VCO namely time domain approach and frequency domain approach.

In this project I use both of approaches to arrive at the given delay-cell design. The phase noise of proposed VCO is shown in fig.5.6. It gives -83.36 dBc/Hz and –100 dBc/Hz phase noise at the 1MHz and 10 MHz offset frequencies respectively at same 2.79 GHz oscillation frequency. Phase noise is defined as the difference between carrier power and noise power. In single stage topology we can reduce noise power by reducing number of stages and thus we can improved phase noise performance.

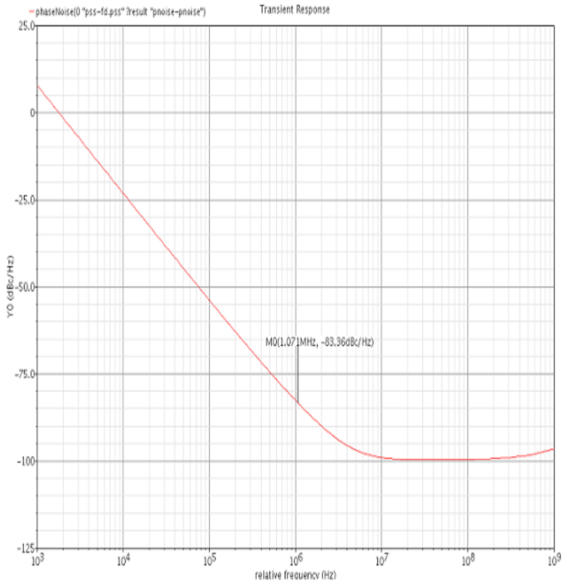

Fig.6.The phase noise of VCO at the oscillation frequency of 2.79 GHz

C. *The oscillation frequency versus the control voltage*

Table I shows the variation in oscillation frequency with respect to control voltage.

Table I

Control Voltage (Vc)	Oscillations Frequency(GHz)
0.70	2.79
0.75	2.70
0.80	2.57
0.85	2.36
0.90	2.08
0.95	1.99
1.00	1.78
1.05	1.49
1.10	1.10
1.15	0.58

Table II: Comparison of Results between other VCO and Proposed VCO

Parameter	[1]	[3]	[4]	[10]	Proposed VCO
Supply Voltage (V)	2.5	3.3	1.2	1.8	1.8
Tuning Range (GHz)	0.66-1.27	0.45-1.15	1.06-1.14	7.40-7.90	0.58-2.79
Phase Noise (dBc/Hz)@ KHz	-106 @600	-100.2	-95.3 @600	-108 @ 1MHz	-83.36 @ 1MHz
Gate length (μm)	0.5	0.35	0.18	0.18	0.18

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IV. Summary and Conclusion

All the simulations were performed on the Tanner modules such as, S-edit, T-spice and W-edit. On Windows platform and using parameter oftsmc018.scs model file. In this paper, we worked single stage voltage controlled oscillator which did not use a spiral inductor. This oscillator can be used for low-voltage low-power applications. The oscillator was based on creating a positive feedback between the sources of the coupled devices. The simulation results showed that the proposed VCO could achieve high oscillation frequency with a good phase noise performance and low power consumption.

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