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Design and Analysis of Low power 6T SRAM Cell

N. L.Vamsi Priya. K.
M.Tech. Student
NCET,Jangareddygudem
priyakece@gmail.com

G. Sravya
Associate Professor
NCET, Jangareddygudem
sravya.ece.jrg@gmail.com

Abstract **— Increasing area overhead is a major design concern in low-power sub-threshold SRAM designs, due to stability considerations. The extensive growth of battery operated devices has made low-power design important in recent years. As electronics are being integrated into portable devices, the demand grows for increased functionality, with reduced size and long battery life. This implies a need to balance ultra-low power with area-efficient design. An obvious way to minimize energy per operation is to decrease V_{DD}. This decreases active power, as well as leakage power, which is affected by DIB. If V_{DD} is decreased too sharply, however, increased delay time causes the power-delay product (PDP) to rise, can be kept minimum if operated in Sub-threshold region. In this paper the advantages of the sub-threshold inverter compared to the conventional strong inversion inverter with 90 nm technology in Cadence is presented. A one-Bit 6T SRAM, sense amplifier, and precharge circuit is designed using HSPICE 45nm technology.**

Keywords **— Sub-threshold region, Power-Delay Product, DIBL, Temperature, SRAM.**

I. INTRODUCTION

In the past few years a tremendous rise in VLSI fabrication has led to increase the densities of integrated circuits by decreasing the device geometries. Such high density circuits support high design complexities and very high speed but susceptible to power consumption. Circuits with excessive power dissipation are more susceptible to run time failures and give rise to reliability problems. The other factors behind the low power design is growing class of personal computing devices, e.g., as portable desktops, digital pens, audio and video based multimedia products and wireless communications such as PDA's and smart cards, etc. These devices and systems demand high speed and complex design functionalities. The performance of these devices is limited by the size, weight and lifetime of portable batteries. Memory design is an integral part in these devices and so reducing the power dissipation in these can improve the system power efficiency, performance, reliability.

II. CONVENTIONAL 6T SRAM CELL

SRAM have experienced a very rapid development of low power, low voltage memory design during recent years due to an increase demand for notebooks, laptops, hand held communication devices and IC memory cards. Due to these concerns limiting power consumption is a must and hence new techniques are being realised to improve energy efficiency at all levels of the design. In this paper an overall analysis has been carried-out for the different SRAM cells at various technologies in respect to stability and leakage power consumption.

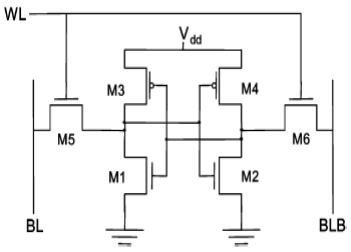

Fig.1. Conventional 6T SRAM

In a 6T cell, variability tolerance is compromised by the conflicting needs of cell read stability and writes ability. Because the same pass-gate devices are used to both read and write the cell, it is inevitable that the two conditions cannot be simultaneously optimized. Just as dynamically modulated power supplies decouple requirements for read and write, such an effect can also be achieved by modifying the cell itself. The 6T SRAM cell stability problems also arise during a write operation to an unselected column when the word line is activated while both bitlines are held high. A situation that produces equivalent bias conditions to a read operation. So, different topologies of SRAM cell have been implemented at various technologies to improve the data stability and leakage power consumption.

III. 8T SRAM CELL

To address the reduced read SNM problem, the read and write operations are separated by adding read access structures to the original 6T cell, thus increasing the transistor count to 8. As the read current does not significantly affect the cell value, then the read stability of the 8T cell is dramatically increased compared with the original 6T SRAM cell. The transistor configuration (i.e. M1 through M6) is identical to a conventional 6T SRAM cell. Write access to the cell occurs through the write access transistors and from the write bitlines, BL and BLB. Read access to the cell is through the read access transistor and controlled by the read wordline, RWL. Figure 3.1 shows that the proposed 8T cell has a higher read SNM, comparing to the 6T SRAM cell. Moreover, the write margin of these two cells (defined as the least bitline voltage required to change the state of SRAM cell) is the same due to the unchanged write configuration. However, for the 8T structure, the read bitline leakage is quite significant especially in the deep submicron/Nano ranges. Since it is not possible to design a high-density SRAM using 8T cells, this conclusion leads to an investigation of other cells.

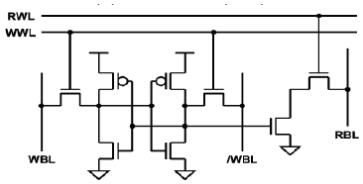

Fig.2. 8T SRAM Cell

IV. 9T SRAM CELL

A 9T structure is proposed in this paper to reduce the power consumption of the SRAM cell and the bitline leakage. Figure shows the proposed 9T SRAM cell. Similarly to the 8T cell of, the configuration from M1 to M6 is unchanged (same as in the 6T SRAM cell). The read SNM margin is maintained by retaining the write access circuit and adding a NMOS transistor (M9) between M7 and M8. As shown in, the leakage current through M7, M8, and M9 can be reduced significantly by the so-called stack effect when M7 and M9 are off.

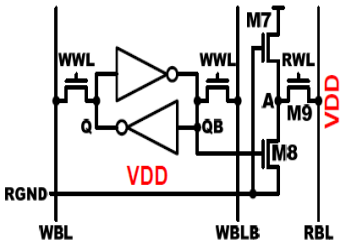

Fig.3. 9T SRAM Cell

V. 10T SRAM CELL

The following figure Shows the schematic of a l0T bitcell that addresses these problems and provides sub-threshold functionality. Transistors M1 through M6 are identical to a 6T bitcell except that the source of M3and M6 tie to a virtual supply voltage rail, VVDD. Write access to the bitcell occurs through the write access transistors, M2 and M5, from the write bitlines, BL and BLB. Transistors M7 through M10implement a buffer used for reading. Read access is single-ended and occurs on a separate bitline, RBL, which is pre charged prior to read access. The wordline for read also is distinct from the write wordline. One key advantage to separating the read and write wordlines and bitlines is that a memory using this bitcell can have distinct read and write ports. Since a 6T bitcell does not have this feature, the l0T bitcell is in some ways more fairly compared to an 8T dual-port bitcell (6T bitcell with two pairs of access transistors and bitlines).

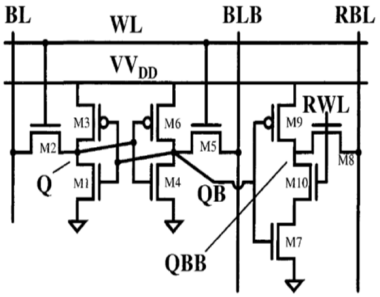

Fig.4. 10T SRAM cell

VI. RESULTS

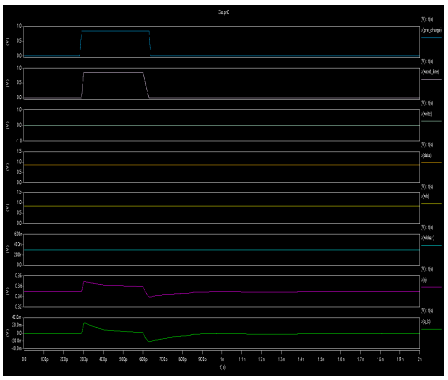

Fig.5. 8T SRAM Write operation

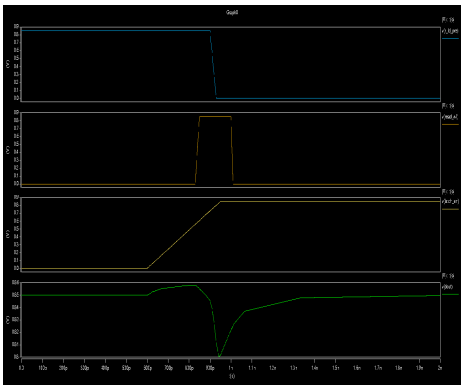

Fig.6. 8T SRAM Read operation

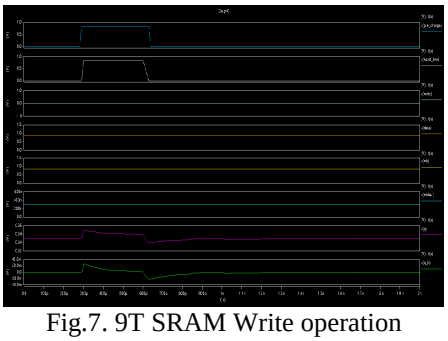

Fig.7. 9T SRAM Write operation

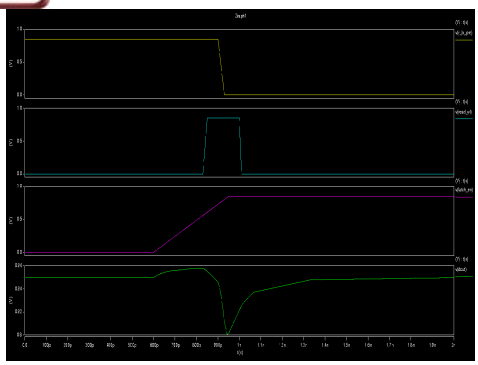

Fig.8 9T SRAM Read operation

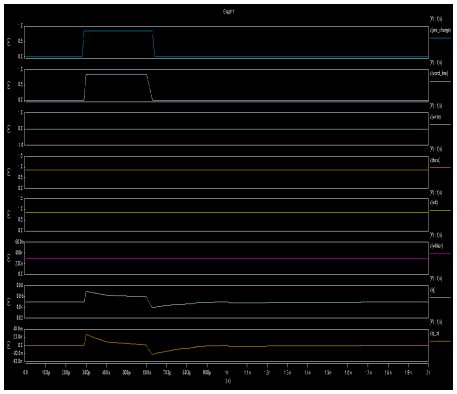

Fig.6.5: 10T SRAM Write operation

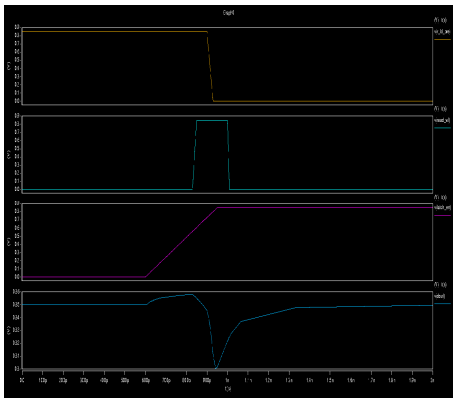

Fig.6.6: 10T SRAM Read operation

VII. CONCLUSION

In this, I made comparisons between different configurations of SRAMs. In all configurations 4T, 6T, 8T, 9T SRAMs SNM is the problem when scaling the voltages. In 10T SRAM we can find optimum power and optimum delay as well as good SNM. 10 T SRAM achieves best stability and low power compared to remaining configurations in 45nm. Read and write operations done for all configurations.

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AUTHOR’S PROFILE

N.L.Vamsi Priya. K.

completed her B.Tech from JNTUH in 2005 and presently pursuing M.Tech. from Nova College of Engineering & Technology, Jangareddygudem.

G. Sravya

completed her M.Tech. from JNTUK and presently working as an Associate Professor in Nova College of Engineering & Technology Jangareddygudem.