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Parametric Optimization of Pulse Latch Shift Register in Deep Submicron Technology

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Abstract **— This paper is base on power and area optimization of shift register which is synchronized with pulse clock. The register is design with pulse clock base latches, this reduces the area of design. The pulse clock generator is design and connected to the group of the latches in several sub shifter registers to increase the data length. The design will implemented on 0.05um technology using MICROWIND layout editor tool.**

Keywords **— Pulse Latch, Shift Register, Level Triggered,**

I. INTRODUCTION

The shift registers are the basic building blocks of memory use in microprocessors, micro controllers, digital signal processors etc. The shift register is design by series connected flip flops which is synchronized with a common edge triggered clock input. This circuit does not require any combination circuit between cascaded flip flops. The edge triggered flip flops are design using more than one latch. Flip flop in VLSI design consumes half of the area and dynamic power due to their redundant transition of internal nodes at the time of both input and output are at the same state. This work is base on the shift register design using latches with pulse clock signal. These pulse latch are design using pass transistor logic base transmission gates. The transmission gate passes the input data towards the output and design with less number of transistors. Thus use of pulse latch in shift register design not only design with less number of latches but also use of transmission gate reduces number of transistors. This paper discusses the design on 50 nm technology with channel size of MOSFET is 0.05um and that of width is 0.125um. This is implemented on MICROWIND layout simulator.

Generally shift registers are not design using latches due to the timing problem. The latches are level triggered and also shows race around condition. The main goal has been to find the smallest set of flip flop topologies to be included in a “high performance” flip-flop cell library covering a wide range of power-performance targets. The shift register in Fig. 1(a) consists of several latches and a pulsed clock signal (CLK_ pulse). The operation waveforms in Fig. 1(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width. But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

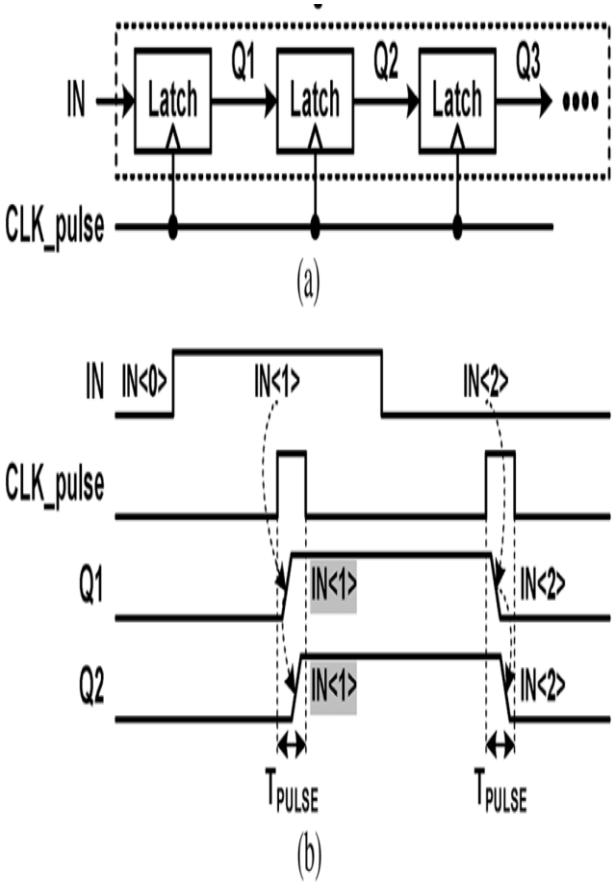

Fig. 1 Shift register with latches and a pulsed clock signal.

II. PROPOSED ARCHITECTURE SHIFT REGISTER

The cascaded master slave base flip flops are mostly used in shift register design with synchronized edge triggered clock signal. While the pulse latch base shift register consist of latches and pulse clock generator circuit. The pulse clock generator is base on 2X4 decoder array type logic and two bit counter. A clock pulse generator circuit is connected to the group of latches and form the chain of sub shift registers. The output of this array generates any one output to logic '1' level depend on input. This output is use as a clock pulse signal for latches in shift register. Thus the use of single pulse latch reduces the area up to 50% as compared to conventional design. This shift register is design using latches. The non-overlap delayed pulsed clock signal is applied on every latch of the cell.

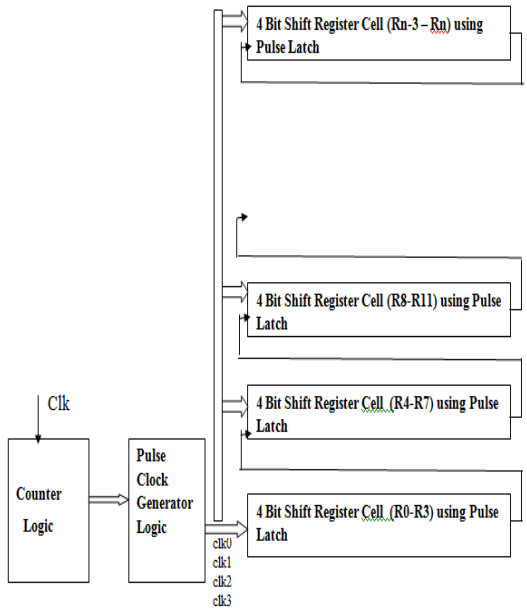

Fig. 2 Block Diagram of Propose Pulse Latch Shift Register.

The pulse clock generator generates clock pulses for the level triggering of latch. The two bit counters output is connected to the two inputs of decoder circuit. The output of decoder generates logic high pulses at its anyone output at one time. These outputs are the connected to the level trigger clock signal of pulse shift register.

The output of pulse clock generator will activates only one latch at one time in a group of series connected latches. This process solves the timing problem of asynchronous behaviour if latches. Thus the activated latch shift its input data towards the next series connected latch. Thus at every clock pulse triggered the data is shifted towards the successive latches. This circuit reduces the number of latches require for shift register design which in turn reduces the area and power dissipation.

III. Related Work

Shift Register Using Pulsed Latches design with seven transistor base cross connected inverter logic of data latch. Delay clock pulse generator circuit is use to synchronized a chain of group of shift registers. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. Their proposed shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches [1].The basic cell of shift register is flip flop. In [2], flip flop is design with adaptive coupled latch circuit. The AC elements composed of a CMOS pass gate are required to overwrite the master latch connected to the input inverters through PMOS pass transistors. When the master latch value is transferred to the slave latch, the AC elements isolate the cross-couple connection in the master latch to make it easier for the master latch to overwrite the slave value [2].

IV. Design Flow

The performance of a flip-flop is qualified by three important timings and delays: propagation delay (Clock-to-Output), setup time and hold time. They reflect in the system level performance of the flip-flops. Setup time and hold time define the relationship between the clock and input data. The design flow shows the simulation and parametric extraction of pulse latch shift register modules. A Schematic is design for clock generator and latch logic. The CMOS layout of this schematic is implemented on MICROWIND lay put simulator tool with design specifications. Design rule checker observe the error in design. The objective associated with design rules is to obtain a circuit with optimum yield in as small as area possible without compromising reliability of the circuit. Then input test pattern is applied on this design for timing simulation.

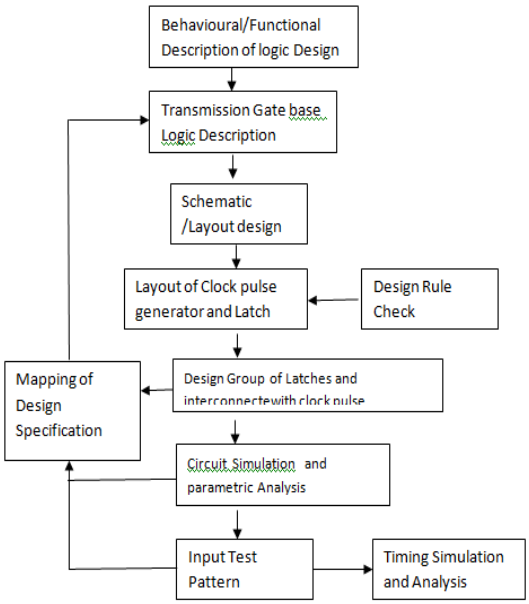

Fig. 3 Design Flow

The layout of the shift register circuit is design by considering the channel length, channel width, VDD, and clock rail. Design rule checking (DRC) and the circuit structure extraction are performed on the layout view of the shift register system. The view extracted from the layout and the original schematic views are compared with the layout versus schematic (LVS) tool simultaneously. During the physical layout design, regularly run DRC and check on the finished blocks.

V. Propagation Delay

Propagation delay (Clock-to-Output) is the time delay after arrival of clock's active edge that output is considered stable. Clock-to-Output equals the time it takes for the output to change after the occurrence of the clock edge. Usually propagation delay differs for low-high transitions and high-low transitions. So propagation delay

of the flip-flop is by definition maximum value of these two delays.

VI. Setup Time

In order to function correctly, the edge-triggered flip-flop requires the input to be stable some time before the clock's active edge. This period is called the setup time of the flip-flop. The data value must remain stable around the time clock signal changes value to ensure that the flip-flop retains the proper value. As setup time may differ for low-high transitions and high-low transitions, setup time is by definition maximum of the values obtained for low-high and high-low transitions

VII. Hold Time

Flip-flop design requires the state of the input to be held for some time after the clock edge. The time after the clock edge that the input has to remain stable is called the hold time. Basically hold time can be negative meaning that data can be changed even before clock edge and still previous value will be stored. Hold time is by definition maximum of the values obtained for low-high and high-low transitions.

In these definitions, propagation delay, setup time and hold time are considered as independent variables. However what happens in reality shows that these parameters are not independent from each other. For instance, propagation delay is strongly related to the data arrival time.

The extended method of sizing of transistors is done in an iterative manner and consists of the following steps.

1. The transistor size of CMOS logic design uses 0.05µm channel length and 0.125µm channel width in 50nm technology.
2. The sub modules are design as per the input output behaviour of truth table and the sub modules are inter connected to form the complete design.
3. The parametric analysis of delay, area and power is done through simulation.
4. Step 3 and step 4 is repeated till a optimized parametric estimation is met. The transistors in the critical path, which produce output results of the transition that causes the maximum Td need to be sized.

VIII. Conclusion

This paper discusses the block diagram and design of pulse latch base shift register. The transmission gate-based flip-flops exhibit the best power-performance trade-off with a total delay (clock-to-output) reduces as compare to conventional flip flops. The use of transmission gate in flip flop design will reduce the number of transistors requirement and also reduces the stray capacitances. The pulse clock generator is design and connected to the group of the latches in several sub shifter registers to increase the data length. The design will implemented on 0.05um technology using MICROWIND layout editor tool.

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