

# Parametric Optimization Speed, Power and Area for Carry Select Adder: A Survey

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**Abstract** – In today’s era the low power and faster adder logic is the major concern area in deep submicron technology. The addition speed is affected due to the time delay of carry signal propagated from one adder to its successive adder circuit. The addition of next two bits is generated only after the previous addition is completed and its carry is propagated for next bit addition. This speed limitation is trade off by the use of carry select addition by generating multiple number of carries and selecting the appropriate carry require for next addition bits. This carry selection is done by multiplexer logic. But this logic increases area of design. This paper discusses the area, power and delay efficient carry select adder (CSLA) design.

**Keywords** – CSLA, RCA, CSKA.

## INTRODUCTION

The speed comparison among the adders shows that the Carry Look Ahead Adder and Carry select Adder is faster and ripple carry adder is having *lesser speed*. While in *area point of view* Ripple Carry Adder had a less area, Carry Select Adders posses a larger area and a Carry Look Ahead Adder is having tradeoff between speed and area complexities. In the carry select adder working the addition of two numbers is done in two ways. In first way two numbers are added with by assuming the previous carry is ‘0’ and in second way two numbers are added with by assuming the previous carry is ‘1’. After this the correct output is selected by knowing the value of previous carry. Its logic equation is

$$S_{i-1:k} = \bar{c}_k S_{i-1:k}^0 + c_k S_{i-1:k}^1$$

$$c_i = \bar{c}_k c_i^0 + c_k c_i^1$$

The major parameter which affects the speed of adder is the carry output. As carry propagate from one adder to the next adder, it slows the addition speed. The basic idea this carry select adder is using the addition of bits in grouping form for considering the carry as both logic ‘1’ and logic ‘0’. After that the sum of logic is decided by seeing the previous carry input. To reduce area, CSLA adder is design using transmission gate. Transmission gate design the adder with less number of transistors [2,3,4].

This logic can be design with Carry Select Adder to get Low Power and Area competence. The designed 32-bit Carry Select Adder compared with the Carry Skip Adder (CSKA) and Regular 32-bit Carry Select Adder. The CSLA is use in various computational systems to improve the problem of carry propagation delay by in parallel

generating multiple carries and then select a carry to produce the sum. Although, the CSLA is not area optimized because it is design with multiple pairs of Ripple Carry Adders (RCA) to produce partial sum and carry in view of carry input  $C_{in} = 0$  and  $C_{in} = 1$ , then the last sum and carry are selected by the multiplexers (mux). The complete work performed by usage of Binary to Excess-1 Converter (BEC) instead of RCA with  $C_{in} = 1$  in the usual CSLA to get lower power consumption The major improvement of this BEC logic comes from the lesser number of logic gates than the n-bit Ripple Carry Adder (RCA). A design of 4-bit BEC and the truth table is shown in Fig.1 and Table 1 respectively [1].

Table.1 : Functional Table of 4-Bit BEC

B [3 : 0]	X [3 : 0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

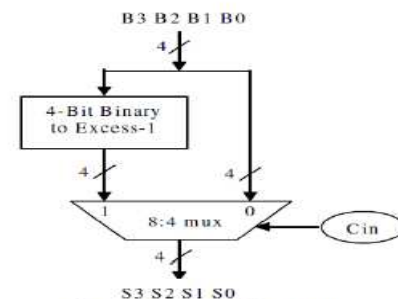


Fig.2. 4-b BEC with 8:4 mux

## Arithmetic Addition

There are various types of adders available depends on their design structure and the logic of addition. Some of these adders commonly used are: parallel adder also called as ripple carry adder (RCA) which is slower in speed due to delay of carry propagation, Carry look ahead adder (CLA) which is faster with area trade off, Manchester chain adder (MCA), Carry save adder etc. The carry propagation delay of ripple carry adder depends on the number of adder cells. Thus its speed performance is affected if number of bits increases for addition. The propagation time, for the addition of two binary numbers using any generic parallel adder, can be speed up considerably if adder uses a Manchester cell in its structure.

The speed trade of ripple carry adder due to carry propagation is overcome by using look ahead carry adder but with compromise of area. The carry select adder

design with faster speed large area compare with ripple carry adder but less area less speed as compare with look ahead carry adder.

*Logic Formulation and Schematic Design*

The CSLA has two units: 1) the sum and carry generator unit (SCG) and 2) the sum and carry selection unit [9]. The SCG unit consumes most of the logic resources of CSLA and significantly contributes to the critical path.

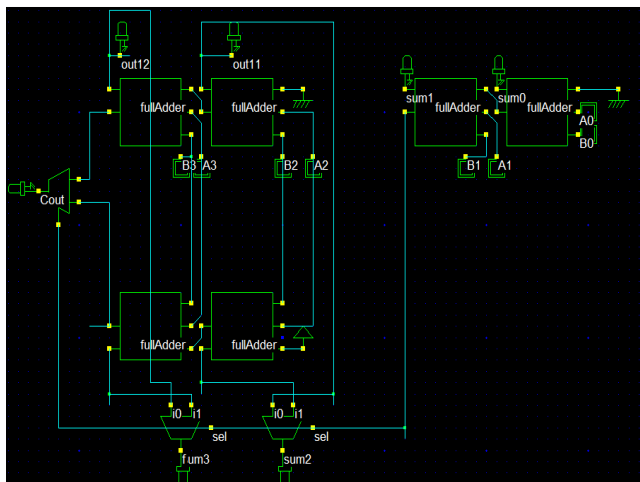


Fig. Schematic Diagram of 4 bit Carry Select Adder

Fig shows the schematic design for two stage two bit ripple adder for design of 4 bit carry select adder. The stage 1 is design using two bit ripple carry adder. In stage 2 a two blocks of 2 bit ripple carry adder is design with assuming that previous carry is '0' or '1'. In this stage, first block is use to add two most significant bit with assuming that the previous carry is '0' and the second block is use to add two most significant bit with assuming that the previous carry is '1'. This design uses 6full adders and 3 two input and one output multiplexers. The carry out bit of first stage ripple carry adder is connected to the selection input of 2X1 multiplexer. If this carry is '1' then it select the output of second stage block of ripple carry adder with previous carry '1' and if this carry is '0' then it select the output of second stage block of ripple carry adder with previous carry '0'.

Fig shows the timing simulation of 4 bit carry select addition. The two least significant bits are added by ripple carry addition. And the carry out of this addition will select the ripple carry addition of next stage. For example lets take the addition of two four bit numbers (1011 and 1111)<sub>2</sub>. The addition of two LSB numbers 11 and 11 gives the two LSB sum of 10 along with carry bit '1'. The ripple carry addition of two most significant (MSB) number gives MSB sum of 01 and 10 for previous carry assuming as '0' and '1' respectively. The result of MSB is decided by the carry bit of first stage addition. Thus the final result of this addition is (11010)<sub>2</sub>.

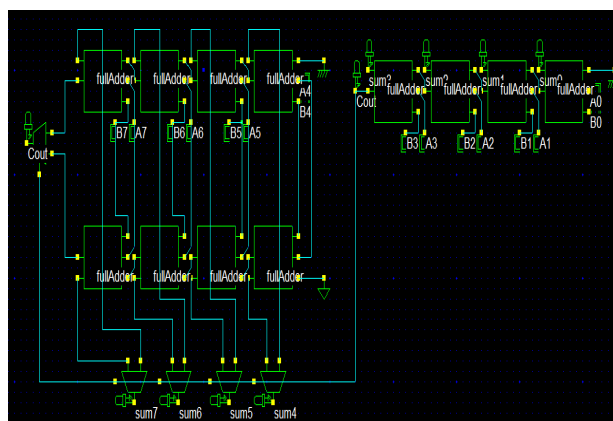
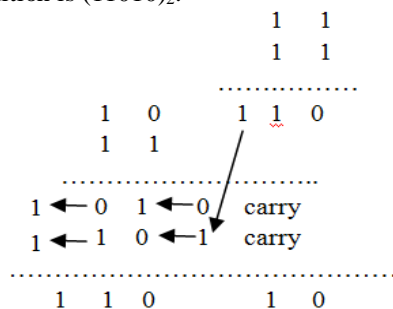


Fig. Schematic Diagram of 8 bit Carry Select Adder

Fig shows the schematic design for two stage four bit ripple adder for design of 8 bit carry select adder. The stage 1 is design using four bit ripple carry adder. In stage 2 a two blocks of 4 bit ripple carry adder is design with assuming that previous carry is '0' or '1'. In this stage, first block is use to add four most significant bit with assuming that the previous carry is '0' and the second block is use to add four most significant bit with assuming that the previous carry is '1'. This design uses 12 full adders and 5 two input and one output multiplexers. The carry out bit of first stage ripple carry adder is connected to the selection input of 2X1 multiplexer. If this carry is '1' then it select the output of second stage block of ripple carry adder with previous carry '1' and if this carry is '0' then it select the output of second stage block of ripple carry adder with previous carry '0' [2,3,4,5].

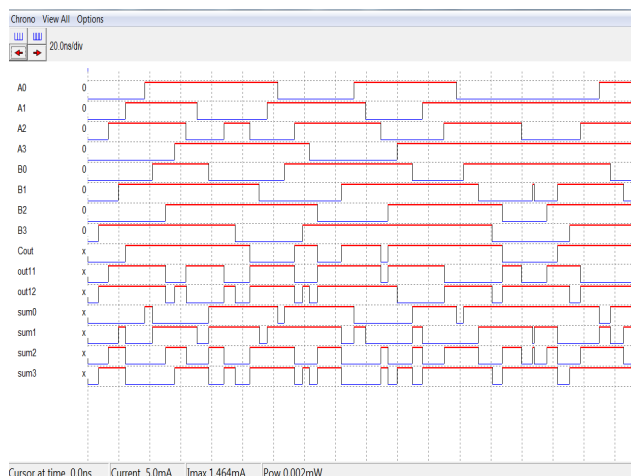


Fig. Timing simulation of 4 bit Carry Select Adder



which is different from the conventional approach. For the addition of multi bit numbers is decompose in a groups and the delay incurred in this addition is equal to the ripple carry delay of parallely executed intermediate stages. The speed of addition is improve but with area trade off.

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