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Study Analysis of Various Low Power Zero Partial Product Bypass Multipliers

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***Abstract* — In today's CMOS VLSI era, power, speed and areas are the main issues of concern. Advances in microelectronic technology have led to more effective and secure communication and embedded intelligence in systems. In particular, to meet the increasing market demand for portable applications, these microelectronic devices consume very low power. Hence low power consumption becomes one of the most important criteria for the fabrication of recent DSP and high performance systems. It is the well known fact that the multipliers are the main power hungry elements of DSP and communication systems. If we can reduce the power consumption of the multiplier block, then we can reduce the power consumption of various digital signal processing chips and communication systems. This type of power efficient multipliers can be developed by reducing switching activities through architecture optimization. Reduction of switching activities through architecture optimization can be done using Bypassing Techniques (Turning of some columns or rows or both in the multiplier array whenever certain multiplier or multiplicand or both bits are zero). This paper presents various power efficient multiplier structures based on Bypassing Techniques. This will help in choosing among power efficient Bypass Multipliers for various portable DSP and communication systems.**

***Keywords* — Switching Activity, Array Multiplier, Row and column Bypass Multiplier, Booth Recording Unit.**

I. INTRODUCTION

The multiplication is an essential arithmetic operation for common DSP and Communication applications, such as filtering and fast Fourier Transform (FFT) . To achieve high execution speed, parallel array

multipliers are widely used. These multipliers tend to consume most of the power in DSP computations, and thus power-efficient multipliers are very important for the design of low-power DSP and Communication systems.[1]

The computation of a multiplier manipulates two input data to generate many partial products for subsequent addition operations, which in the CMOS circuit design, require many switching activities.[2] Thus, switching activities within the functional units of a multiplier account for the majority of the power dissipation of a multiplier, as given in the following equation:

$$P_{SWITCHING} = \alpha C V_{dd}^2 f_{clk} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Where α is the switching activity parameter, C is the loading capacitance, V_{dd} is the operating voltage, and f_{clk} is the operating frequency. αC can also be viewed as the effective switching capacitance of the transistors' nodes on charging and discharging. Therefore, minimizing switching activities can effectively reduce power dissipation without impacting the circuit's operational performance.[3]

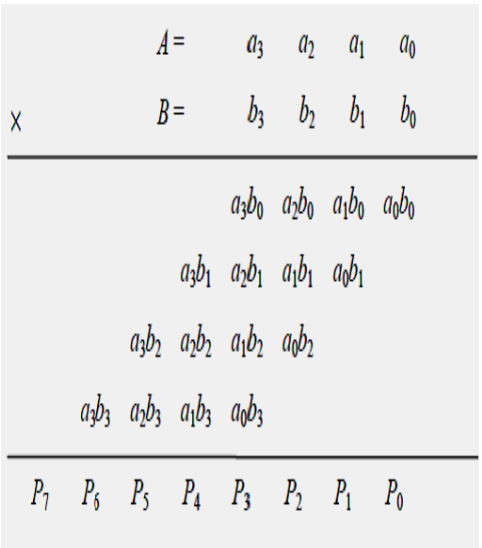
This paper presents various low power parallel multiplier, in which switching activities are reduced through architecture optimization, based on **Bypassing Techniques**. This paper is organized as follows. In the next section we give the information about the basic parallel array multiplier structure. Subsequent sections threw light on possible bypassing multiplier structures, and last section gives the comparison of these structures based on power consumption and area overhead.

II. BASIC PARALLEL ARRAY MULTIPLIER STRUCTURE

For the multiplication of two unsigned n-bit numbers, the multiplicand $A = a_{n-1}\, a_{n-2} \ldots a_0$ and the multiplier $B = b_{n-1}\, b_{n-2}, \ldots, b_0$, the product $P = P_{2n-1}P_{2n-2}, \ldots, P_0$, can be represented as the following equation:

$$P = P_0\, P_1 \ldots P_{2n-1} = \sum a_i\, b_j\, 2^{(i+j)} \quad \ldots\ldots (2)$$

To achieve the high-performance demand in DSP applications, the structure of a parallel array multiplier is widely used and a typical array implementation of such a parallel multiplier is the Braun's design as shown in Fig1.



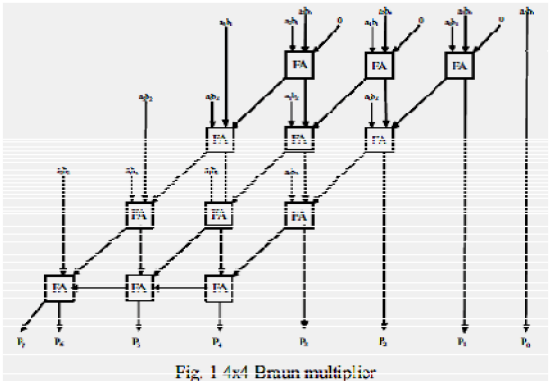


Fig. 1 4x4 Braun multiplier

Drawbacks:

- The number of components required in building the Braun Multiplier increases quadratically with number of bits(a m x n requires mx(n-1) adders & mxn gates). This makes Braun Multiplier **inefficient.**
- The adders of this multiplier performs summation of zero partial products also and, as a result, exhibit **redundant signal switching**. The increased activity in the internal nodes results in **unnecessary power dissipation**.[4]

III. Row Bypassing Multipliers

Bypassing with reference to multiplier means **turning off** some columns or rows or both in the multiplier array whenever certain multiplier or multiplicand or both bits are zero. This Row Bypassing technique is based on number of zeros in the multiplier bits. In this multiplier operation of some of the rows of adders in the basic multiplier array are disabled during operation ,to save the power. If bit B_j of multiplier (B) is 0, all products in row j (A_iB_j for $0 \le i \le n-1$) are zero, and thus the addition in the corresponding row can be bypassed which results in reduction of power. A straightforward approach to design this type of multiplier is to design an Full Adder (FA) that consumes less power.[1] Following figure 2 shows the structure of FA used in this case & the structure of row bypassing multiplier is shown in Figure3.

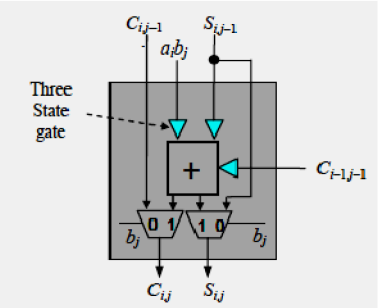


Fig. 2. The Modified FA Cell

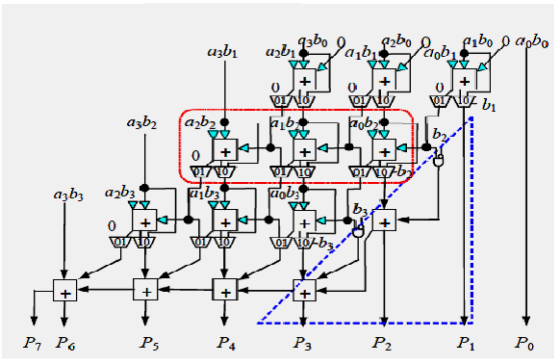


Fig. 3. A 4X4 Row Bypassing Multiplier

Drawback :-Additional correcting circuitry

For example, let b2 be 0 in above figure. In this case, the CSA in the second row (enclosed by the red circle) can be bypassed, and the outputs from the first row are fed directly to the third row CSA. However, since the rightmost FA in the second row is disabled, it does not execute the addition and thus the output is not correct. In order to remedy this problem, extra circuit must be added, and these elements locate in the triangle area in Figure 3.

IV. Column Bypassing Multipliers

As the Row Bypass multipliers are suffered from having extra correcting, a new low power bypassing multiplier design structure was developed, known as **Column Bypassing Multiplier**. In this technique, instead of bypassing the rows of adders during working, the operations in a column can be disabled if the corresponding bit in the multiplicand is 0, to save the power. This technique is totally depended on the number of zeroes in the multiplicand bits, unlike the row bypass multiplier. There are two advantages of this approach. First, it eliminates the extra correcting circuit as shown in Figure 3. Second, the modified FA is simpler than that used in the row-bypassing multiplier, as shown in Figure 2. The figure 4 shows the modified FA cell for this technique, and the figure 5 shows 4x4 Column Bypass multiplier.[1]

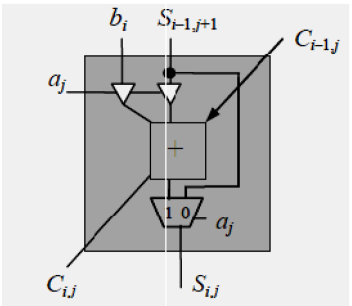


Fig. 4. The Modified FA Cell For Column Bypass Multiplier

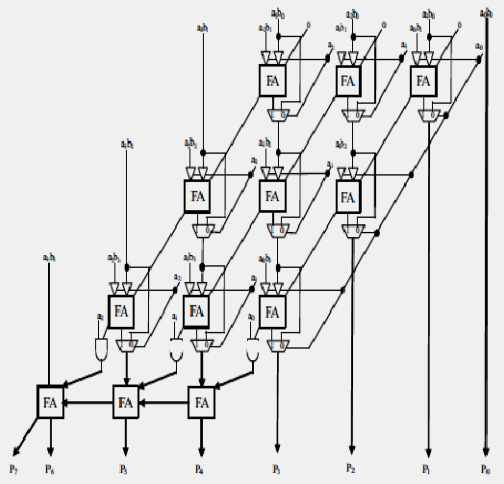


Fig. 5. A 4X4 Column Bypassing Multiplier

V. Improved Column Bypassing Multipliers

The above researches have following adverse effects: -

- ¾ Previous designs use tri-state buffers to retain or freeze the data at input nodes when bypassing occurs. These data, however, will degrade with time due to leakage current problem. When a sufficient voltage drop (greater than a threshold voltage) is reached, it will cause simultaneous conduction of both P- and N- logic sections and thus lead to unnecessary DC power consumption.
- ¾ The incurred tri-state buffers and multiplexers give rise to considerable circuit overhead.
- ¾ The carry logic in column bypassing scheme are neither input latched nor output bypassed to save the circuit overheads of one tri-state input buffer and one 2:1 output MUX. The unreined and erroneous carry signals are finally gated to zero at the bottom of the adder array before being fed into the carry propagation adder. This implies not only extra gating logic but also unnecessary switching activities in carry logic. These can be effectively by improved column bypassing technique given below.

To achieve power saving by column bypassing scheme, two mechanisms must be implemented, i.e. signal multiplexing (between a bypassing signal and an evaluated signal) and evaluation suspension (of the bypassed full adder). In the improved column bypassing structure, C2MOS circuitry is adopted to serve both purposes. The corresponding designs are shown in Figure 6 & 7, respectively. The basic idea is to suspend logic evaluation rather than to suspend (or retain) input signals.[5]

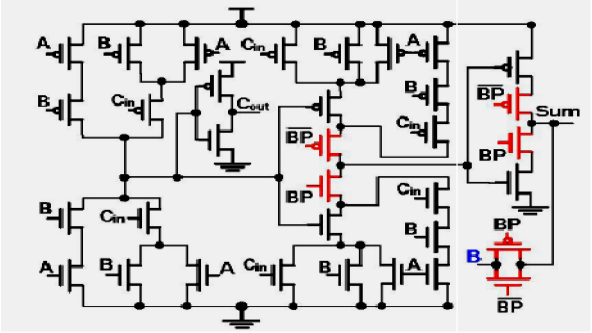


Fig. 6. Design I C2MOS full adder design for Column Bypassing scheme

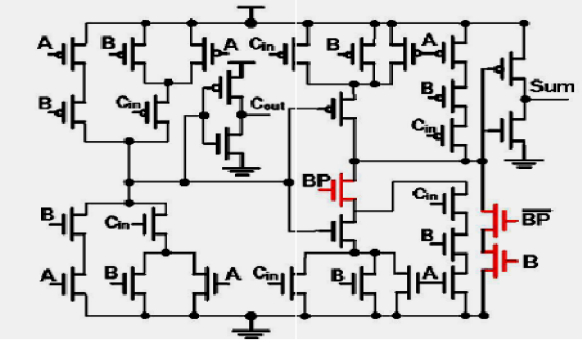


Fig. 7. Design II - N-logic guarded full adder design for Column Bypassing Scheme

In the first design shown in Figure 6 , the input tri-state buffers are removed. Instead, the logic is implemented in C2MOS and the evaluation is guarded by a bypass signal (active low). This can avoid the DC power consumption problem provided the voltage levels of input signals are degraded. In second design as shown in Figure 7, the circuit complexity of the bypassing scheme is further simplified at the trade off of bypassing efficiency.

VI. 2-D Multiplier With Row and Column Bypassing

In this multipliers, the addition operations in the (i+1)-th column or the j-th row can be bypassed for the power reduction if the bit, ai, in the multiplicand is 0 or the bit, bj, in the multiplier is 0. Here the carry result in the previous row is integrated in the 2-dimensional bypassing process. Therefore, the addition operation in the (i+1, j) FA can be bypassed in this bypassing multiplier if the product, aibj, is 0 and the carry bit, ci,j-1, is 0, that is, as the product, aibj, is 1 or the bit, ci,j-1, is 1, the addition operation in the (i+1, j) FA can be executed[6]. 4X4 2-D multiplier with row and column bypassing is illustrated in Fig. 8.

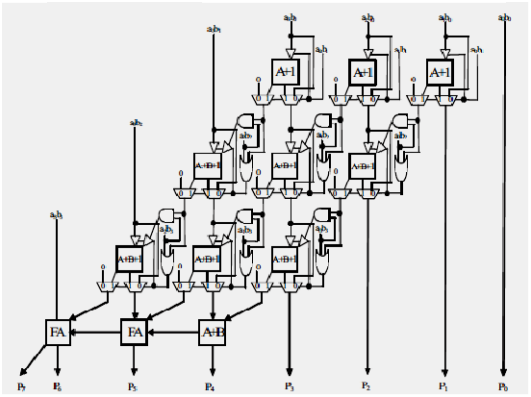


Fig. 8. A 4x4 2-D multiplier with row and column bypassing

VI. Column Bypass Multiplier With Booth Re ording Unit

Sanjiv Kumar Mangal [7] et.al, found one limitation of Column Bypassing Technique. In this technique, number of working columns of the adders depends on the number of ones in the multiplicand. If the multiplicand is 8 bit in length as 11111111 then all the full adders in all the columns will get switched and consume more power. Hennce a new scheme was developed by him, in which multiplicand is represented as 10000000*b* where *b* is -1, which will switch only two columns and ultimately reduces the switching and thus power dissipation.

Higher power reduction can be achieved if the multiplicand contains more number of 0.s than 1.s. In this approach we propose Binary / Booth Recoding Unit which will force multiplicand to have more number of zeros. The advantage here is that if multiplicand contains more successive number of one's then booth-recoding unit converts these ones in zeros. This structure is shown in below diagram 9.

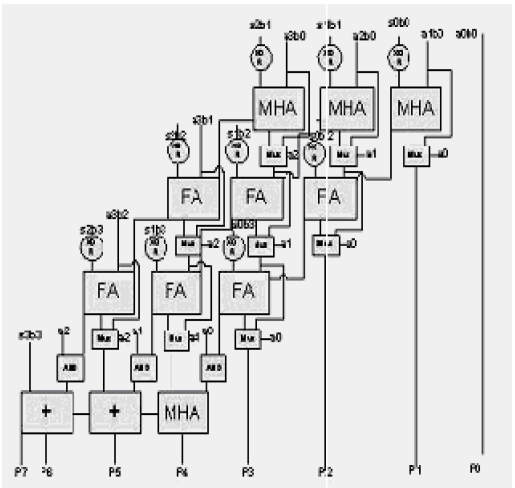


Fig. 9. A 4x4 Column Bypass Multiplier with Booth Recording Unit

VII. Comparison

Multiplier (4X4)	Power Consumption (%) [Simulation on Xilinx 10.1]	Area Overhead Of Transistors (%)
Basic Array	100	100
Row Bypassing	108	169.75
Column Bypassing	87.43	140
2D with Row and Column Bypassing	70.25	120.15

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