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Study of Minimization of Power Dissipation Techniques used in SRAM Cell

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***Abstract* — Power dissipation is the main problem associated with portable devices [1]. Designers are always tried to design the circuit in such way that they can reduce the power as small as possible. Power dissipation, speed and chip area are the three parameters by which we can describe the flexibility of the circuit. Switching speed and power dissipation is the key feature of any memory circuit. If we want to increase the switching speed of the memory circuit than obviously we have to compromise with chip area.**

In this paper we will focused on some method by which the power dissipation can be reduced. Section 1 covers the background detail section 2 describes the various source of power dissipation and its remedy section 3 describe the methods used for power reduction and we will mainly focused on third approach and finally section 4 concludes the paper.

***Key Words* — Power dissipation, SRAM, Threshold voltage, VLSI.**

I. INTRODUCTION OF SRAM

Semiconductor memories can be broadly classified into two groups; read only memory and random access memory. The SRAM is fall into the category of random access memory, where the content of the memory can be accessed randomly. A graph of semiconductor memory organization is shown in figure 1. Memories can also be classified on the basis of access time, function and size. SRAMs basically come in two different flavors: synchronous and asynchronous. Synchronous SRAMs are devices that are synchronized with an external signal called a clock. The device will read and write information into the memory only on particular states of the clock. The particular state of interest is when the clock switches, i.e., when it goes from either LOW-to-HIGH (“rising edge”), or from HIGH-to-LOW (“falling edge”).

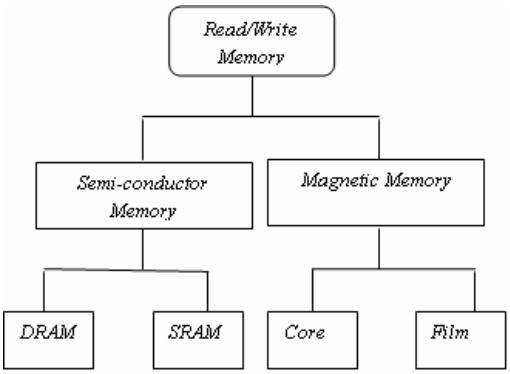

Fig.1. Memory Organization

An asynchronous SRAM, on the other hand, does not depend on the state of a clock. Memories are classified as semiconductor memories and magnetic memories. RAMs are of two types, static and dynamic. Circuits similar to basic D flip-flop are used to construct static RAMs **(**SRAM**s)** internally.

1.1 *Types of SRAM*

SRAM. as its name implies, static, meaning as long as power is applied to the cell it will remember its contents (unlike DRAM). The basic cross-coupled inverter latch is used to design SRAM cell. Classification is done based on their functioning and the type of transistors used, according to memory size, single density or DDR if SRAMs are used in packs (a 4 pack is a quad).

On the basis of functionality SRAM is classified as synchronous and asynchronous. Asynchronous SRAM has a sequential pattern of READ and WRITE operation; while the synchronous SRAM has

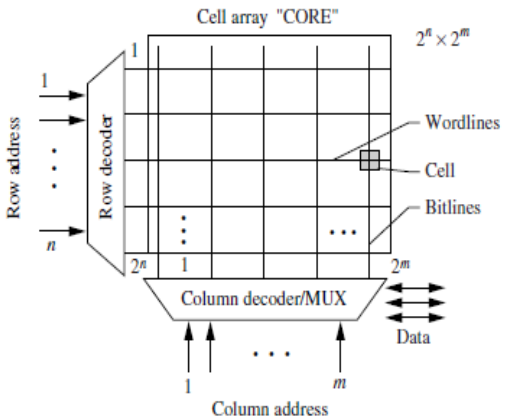

Fig. 2. Structured Memory Organization.

an overlapping READ and WRITES operation. SRAM can also be classified on the basis of number of transistor used as 4T SRAM, 6T SRAM, and 8T SRAM.

1.2 *Memory Peripheral Circuitry*

Peripheral circuitry is used to recover both speed and electric integrity. Many devices are used in periphery of SRAM. The peripheral circuitry also gives the facility of direct access of memory. Content of the memory can be easily accessed by peripheral circuitry. Certain interfacing units are used to make a communication between memory and its peripheral circuitry.

- *The address decoder:* whenever memory allows for random address-based access, the address decoder must be present. They have impact on power dissipation.
- *Sense amplifier:* sense amplifier plays a major role in functionality, performance and reliability of memory circuit. It is used for amplification, delay reduction and signal restoration.
- *Voltage references:* most of the SRAM require some form of on-chip voltage generation. The operation of a sophisticated memory requires number of voltage references and supply levels, including the boosted word-line voltage, half V_{dd} and negative substrate bias.

II. SOURCE OF POWER DISSIPATION IN SRAM

Power reduction is the main concern of many designers. Before moving on the reduction methods first we shall focus on what are factors that cause the power dissipation and how it can be reduced?

Power dissipation has become an important consideration due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances.

There are two types of power dissipation occur in SRAM: dynamic power dissipation, static power dissipation and sub-threshold channel leakage [2]. Dynamic power dissipation can be further classified as short circuit power and power Consumption during switching. Traditionally, the static component of power consumption has been negligible in static CMOS. But when we reduce the dimension of the circuit than static power is taken into account.

The second source of leakage current is the sub- threshold leakage through a MOS device channel. Even though a transistor is logically turned off, there is a non-zero leakage current, through the channel at the microscopic level. This current is known as the sub-threshold leakage because it occurs when the gate voltage is below its threshold voltage. Some of the common methods for power reductions are [3]:

- Capacitance reduction of word- lines and number of cells connected to them, data line, input output lines and decoder.
- DC current reduction, by using a new pulse operation technique.
- AC current reduction by using new decoding techniques. (Multi-stage static CMOS decoding).
- Reduction in operating voltage.
- Leakage current reduction.

These are some common methods generally adopt by designer while designing a power efficient circuit. But some of the drawbacks are also associated with all above methods, such as increment in chip area or decrement in switching speed.

III. POWER REDUCTION TECHNIQUES

Here I describe some of the methods by which power can be reduced and also we can enhance the switching speed. Methods for power reduction are mentioned below.

- Power reduction by using bit-line charge recycling
- Power reduction based on segmented virtual ground
- Low power SRAM design using charge sharing technique
- Power reduction using current sense amplifier

3.1 *Power reduction using bit-line charge recycling*

Charge-recycling SRAM (CR-SRAM) is based on the hierarchical bit-line architecture and the bit-line charge-recycling

Technique. It can recycle the charge in bit lines during both read and write operations, whereas the conventional charge-recycling SRAM. CR-SRAM not only reduces the read power by using the charge-recycling read operation, but also it does not have the power and delay overheads due to the read-to-write mode change of the conventional charge-recycling SRAM With the hierarchical bit line, the CR-SRAM

performs bit-line charge-recycling without static noise margin degradation. Therefore, it can significantly reduce both read and write powers with good reliability [4]. Figure 3 gives the conceptual detail of CR-SRAM architecture. The CR-SRAM reduces the write and write powers by recycling the charge through N BLs. The swing voltage and power of BLs are reduced to 1/N and $1/N^2$, recepectively. To perform the BL charge recycling without SNM degradation, the CR-SRAM utilizes the HBL architecture composed of a BL and several SBLs.

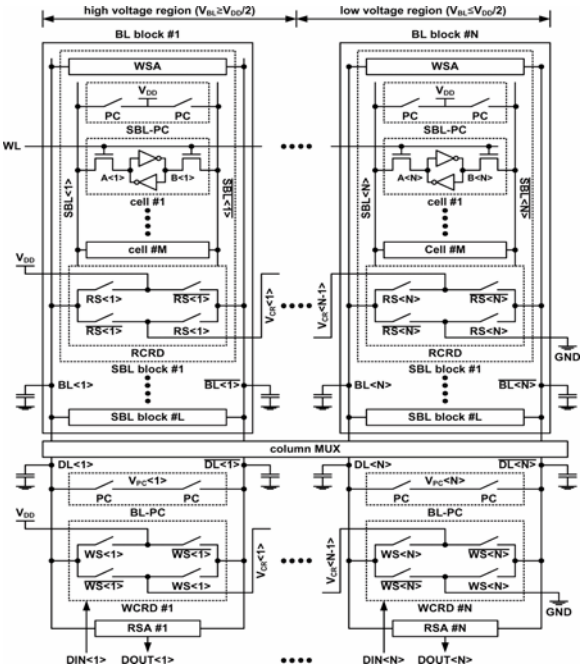

Fig. 3. Simplified architecture of CR-SRAM

3.2 *Power reduction based on segmented virtual ground.*

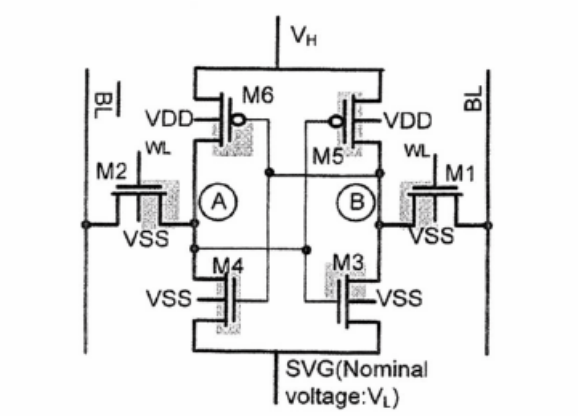

Fig.4. *SRAM with virtual ground*

Figure 4 shows an SRAM cell featured with a virtual ground. Reduction of the write power consumption has been successfully implemented using virtual grounding method. In these schemes, the voltage swing of the bit-lines is reduced significantly by reducing the write noise margin of the cell. Reduction of the write noise margin is achieved by reducing the cell supply voltage during the write operation which results in the destruction of the data stored in a cell. During the read operation, however, the supply voltage increases to provide sufficient overdrive for discharging the bit-line. This scheme, however, drives the non-accessed neighboring cells on the shared source line to an unstable floating region during the write operation, destroying the data of the words located on the same row. This effect limits the application of this technique to high bandwidth applications in which one row represents only one word. The scheme offers low power, low energy consumption in both dynamic and static perspectives. Low dynamic power methods are mostly based on reduction of the signal swings over the bit-lines. Reduction of the bit-line pre-charge voltage reduces the power dissipation in both in and writes operations. This method has been utilized in at the expense of noise margin degradation.

3.3 *Low power SRAM design using charge sharing technique*

The dynamic power of SRAM is dissipated mainly by charging and discharging of the highly capacitive lines. The largest capacitive element in SRAM is bit-lines because a number of cells connected to it. More than 50% of the total dynamic power is consumed by driving the bit-lines. Therefore, reducing bit-lines dynamic power has a significant impact on the total SRAM power-consumption. Due to bit-lines full swing nature in write cycle, therefore, reducing bit-lines voltage swing is an effective way to decrease the power dissipation. Several design techniques such as half swing scheme [7], current mode write operation and sense amplifying memory cell design have been proposed to reduce bit-lines voltage swing[8][9][10]. But those methods not considering the bit-lines of unselected memory cell connected the enabled word-line. Simulation result shows those memory cells bit-lines dynamic power consumption is great.

In order to reduce those unnecessary bit-lines dynamic power, a new SRAM design technique, which adopt charge sharing scheme to reduce bit-lines swing. Compared to conventional SRAM, in write cycle this low bit-lines swing (LBS) SRAM can retain bit-lines full supply-voltage nature and reduce unnecessary bit-lines voltage swing, it greatly reduce bit-lines dynamic power.

3.4 *Power reduction using current sense amplifier*

In this method SRAMs are used with current sense amplifier. Figure 5 shows the SRAM with current sense amplifier.

The scheme has lower power consumption and a higher sensing speed than those of recently proposed. The sense amplifier mainly used to improve the switching speed of the SRAM. In convention SRAM due to large word-line capacitance the switching speed suffers, but when we use a sense amplifier the switching speed improve significantly. Two operating periods of the proposed SRAM are defined below.

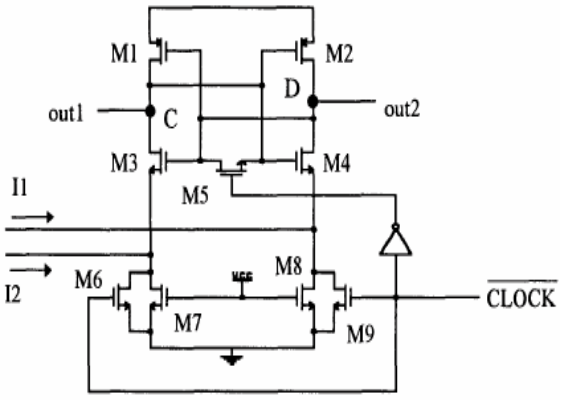

Fig. 5. SRAM with current sense amplifier

3.4.1 *Equalizing period*

In equalization period, M6 and M9 turn off, small size transistor M7 and M8 are the load transistors of sense amplifier. Because of the high load resistance caused by the small size transistors, the DC current flowing through the sense amplifier is reduced. Since the sense amplifier dissipates little power in its sensing period, the whole power consumption of sense amplifier decreases apparently with the equalization current reducing.

3.4.2 *Sensing Period*

In sensing period, large size transistors M6 and M9 turn on so that the amplifier has a high current draining capability to enhance the sensing speed. In addition, the higher load resistance in equalization period conduces to constitute a bigger voltage difference between nodes C and D, which is caused by the differential current signals I1 and 12, at the beginning of sense operation. This is another speed enhancing factor for the proposed sense amplifier.

For SRAM cell, the size of load device is the sum of M6 and M7, or the sum of M8 and M9.

CONCLUSION

In this paper, the latest developments in low-power circuit techniques and methods SRAMs were reviewed. All major sources of power dissipation in these memories were analyzed. Key techniques for drastic reduction of power consumption were identified. These are: capacitance reduction, very low operating voltages, DC and AC current reduction and suppression of leakage currents. Experimental circuits operating at these voltage levels slowly start to emerge in all types of memories. However, there is no universal solution for any of these designs and many challenges still wait for memory designers.

REFERENCES

[1] Low power design an SRAM cell for portable devices. By Prashant Upadhyay, Mr. Rajesh Mehra, Niveditta Thakur. IEEE-2010

[2] Asymmetric SRAM- Power Dissipation and Delay by Ashish Siwach and Rahul Rishi Ijcem 2010.

[3] A low-power SRAM using hierachical bit line and local sense amplifiers, *IEEE J. Solid-State Circuits*, Vol. 40, 2005.

[4] A Low-Power SRAM Using Bit-Line Charge-Recycling for Read and Write Operations." *IEEE J. Solid-State Circuits*, 2010

[5] Low Power SRAM Design Using Charge Sharing Technique" Gu Ming, Yang Jun, Xue Jun *IEEE 2009.*

[6] Current mode technique for high speed VLSI circuit with application of current sense amplifier for CMOS SRAM" IEEE 1991.

[7] K.W.Mai, IEEE J. Of SSC, 33, 11, 1659 (1998).

[8] Jinn-Shyan Wang, IEEE J. of SSC, 35, 1, 119 (2000).

[9] Hizuno, IEEE J. of SSC, 31, 4, 552 (1996).

[10] K.Kanda, H.Sakurai, IEEE J. of SSC, 39, 6, 927 (2004).

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