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Impact of MOSFET Short Channel Characteristic on Digital Circuit Operation

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Abstract — **The design of high density chips in MOS VLSI technology requires that the packing density of MOSFETs use in circuits is as high as possible and consequently, that the transistor are as small as possible. The reduction of the size i.e. dimensions of MOSFETs can change the MOSFET characteristic. In this paper we will examine in detail the non ideal effects on MOS characteristic. These are mainly due to the limitation impose on electrons drift characteristic in the channel and the modification of the threshold voltage due to the shortening channel length. The major short channel effects include the wear-out mechanisms of time dependent dielectric breakdown (TDDB) of gate dielectrics, Threshold voltage and body effects, hot carrier injection (HCI), negative bias temperature instability (NBTI), drain punch through and channel length modulation etc.**

Keywords – **MOSFET, Transistor, Short Channel Characteristic.**

I. Introduction

The basic MOS transistor structure could be scaled to smaller physical dimensions. One could postulate a "scaling factor" of , the fractional size reduction from one generation to the next generation, and this scaling factor could then be directly applied to the structure and behavior of the MOS transistor in a straightforward multiplicative fashion. For example, a CMOS technology generation could have a minimum channel length Lmin, along with technology parameters such as the oxide thickness tox, the substrate doping NA, the junction depth xj, the power supply voltage Vdd, the threshold voltage Vth, etc.

II. Short Channel Effects

2.1 Channel length modulation:

Biasing the gate by coupling the gate voltage to the input reduces Vt by aiding the onset of snapback through increased drain current. Fig 2 shows the I-V characteristic for the transistor for different variable gate voltages. The current is zero for gate voltage below Vt. For higher gate voltage , current increases linearly with Vds. As Vds reaches at the saturation point Vgs- vt, current roll off and eventually become independent of Vds When the transistor is saturated, the MOSFET is a perfect current source and junction between drain and body forms depletion width which reduces channel length. Shorter channel length results in higher current[3],[4],[7].

2.2 Threshold Voltage and Body Effect

The threshold voltage V_{th} for a nMOS transistor is the minimum amount of the gate-to-source voltage V_{GS} necessary to cause surface inversion so as to create the conducting channel between the source and the drain. For $V_{GS} < V_{th}$, no current can flow between the source and the drain. For $V_{GS} > V_{th}$, a larger number of minority carriers (electrons in case of an nMOS transistor) are drawn to the surface, increasing the channel current. However, the surface potential and the depletion region width remain almost unchanged as V_{GS} is increased beyond the threshold voltage[1].

The physical components determining the threshold voltage are: work function difference between the gate and the substrate, gate voltage portion spent to change the surface potential, gate voltage part accounting for the depletion region charge, gate voltage component to offset the fixed charges in the gate oxide and the silicon-oxide boundary[1][2].

2.3 HCI AND NBTI

With the geometric scale down, HCI and NBTI problems become worse. In the channel of the MOS, a high electrical field is created close to the drain. The gate oxide thickness is also reduced to allow low threshold voltages. When the channel is conducting , the high electrical field close to the drain generates an injection of hot carriers into the (SiO2) gate oxide layer[2],[6]. This inserts charges in the oxide by trapping carriers (electrons and holes). These carriers can cause permanent changes in the oxide-interface charge distribution. This can also degrade the device's drain current capability. The accumulation of trapped charge will lower saturation current Idsat, cause Vt drift, lower the linear region transconductance, and degrade the subthreshold slope. As the geometry scales down, these problems become worse. Some IC manufacturers have already reported HCI problems for 0.5 um processes.

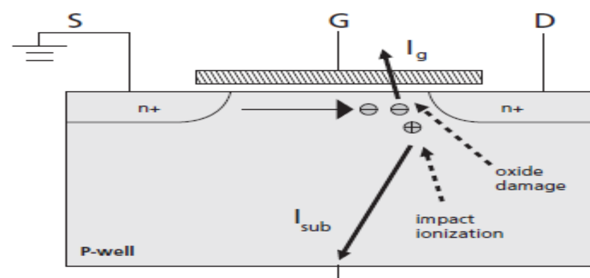

Fig.1. HCI and NBTI

2.4 Drain punch-through:

In a MOSFET device with improperly scaled small channel length and too low channel doping, undesired electrostatic interaction can take place between the source and the drain known as *drain-induced barrier lowering* (DIBL) takes place. This leads to punch-through leakage or breakdown between the source and the drain, and loss of gate control. One should consider the surface potential along the channel to understand the punch-through

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phenomenon. As the drain bias increases, the conduction band edge (which represents the electron energies) in the drain is pulled down, leading to an increase in the drain-channel depletion width.

In a long-channel device, the drain bias does not influence the source-to-channel potential barrier, and it depends on the increase of gate bias to cause the drain current to flow. However, in a short-channel device, as a result of increase in drain bias and pull-down of the conduction band edge, the source-channel potential barrier is lowered due to DIBL. This in turn causes drain current to flow regardless of the gate voltage (that is, even if it is below the threshold voltage (V_{th}).

III. What is Layout

Integrated Circuit (IC) Layout or mask design is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit. In other words, Layout is the process by which a circuit *specification* is converted to a *physical implementation* with enough information to deduce all the relevant physical parameters of the circuit. A layout engineer's job is to place and connect all the components that make up a chip so that they meet all criteria. Typical goals are performance, size, and manufacturability.

3.1 The Role of Laypout in Design:

From a computer scientist's point of view, the layout process seems familiar enough. We are given a piece of *source code*, this time usually in terms of a circuit diagram, and we want to compile it to an *object code*, the physical layout of the circuit. The layout step is the last major step in the design process before testing and fabrication; it is the step which reveals to the designer all the subtle electrical characteristics of the clean and logical digital systems[5],[6],[7].

Results and Conclusion

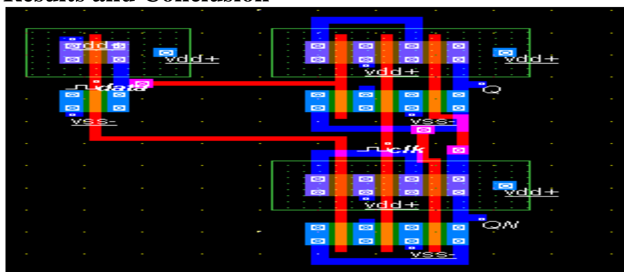

Fig.5. Delay latch with 2 lamda technology

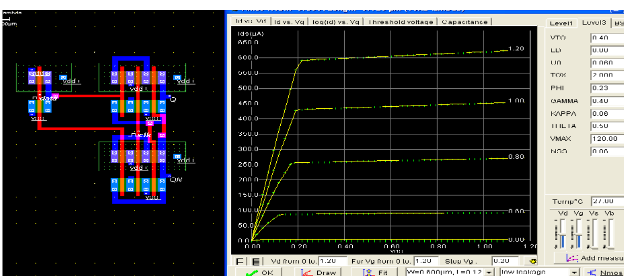

Fig.2. Layout design for D Latch

The potential difference between E_I and E_F for the p-substrate is

$$ØF= KT/q \ln(NA/ni)$$
$$= 1.38*10^{-23} *300/1.6*10^{-19} \ln (10^{14}/1.5*10^{10})$$
$$= 0.228 \text{ V}$$

$$Cox= ox /tox = 3.9*80854*10^{-14}/ 200*10^{-8}$$
$$= 1.7256*10^{-7}$$

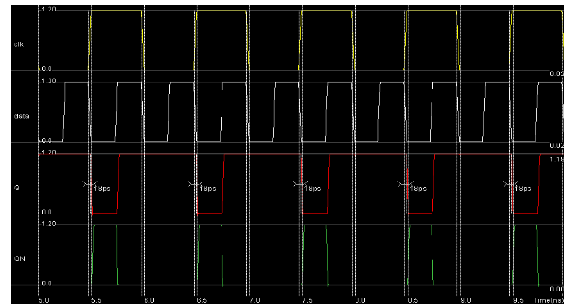

Fig.3. Delay latch with 2 lamda technology output wave

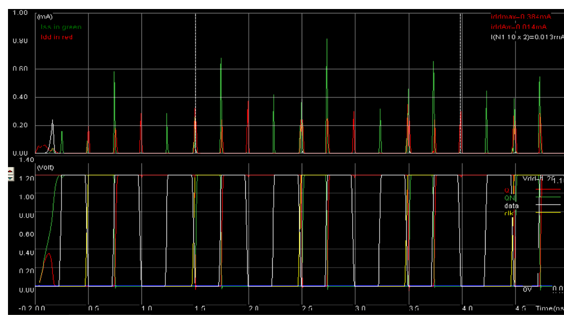

Fig.4. Delay latch with 2 lamda technology output wave

The depletion charge density at V_{SB} =0 is

$$Qdep = (4 \ si \ q \ Na \ ØF)^{1/2}$$
$$= (4*11.7*8.854\text{-}10^{-14}*1.6*10^{-19}*10^{14}*0.228)^{1/2}$$
$$=3.8879*10^{-9}$$

The oxide-interface charge density is

$$ØF = q \ Nox$$
$$=1.6*10^{-19}*4*10^{10} \text{ C/cm}^2$$
$$=6.4*10^{-19} \text{ C/cm}^2$$

Combining the four components, the threshold voltage can now be computed as

$$Vt = Øms\text{-} ØF/Cox + 2ØF +Qdep/Cox$$
$$=0.4 \text{ V}$$

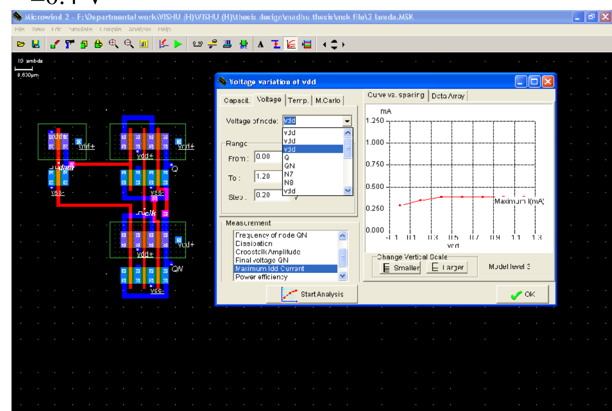

Fig.6. Delay latch with 2 lamda technology output wave maximum Idd current

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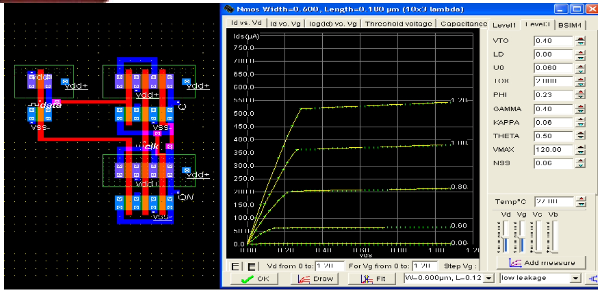

Fig.7. Delay latch with 3 lamda technology

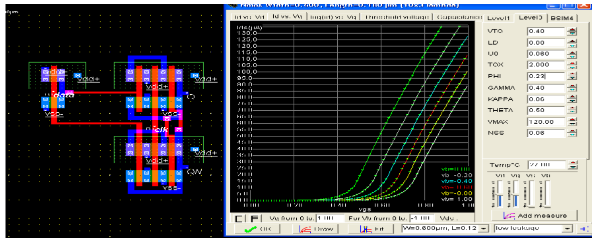

Fig.8. Delay latch with 3 lamda technology Ids-Vgs characteristic

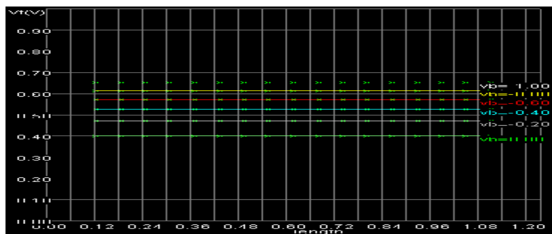

Fig.9. Delay latch with 3 lamda technology Vt characteristic

The threshold voltage V_{th} does vary with the voltage difference V_{sb} between the source and the body (substrate). Thus including this difference, the generalized expression for the threshold voltage is reiterated as

$Vt = Vt0 + (2\ s\ q\ Na)^{1/2} / Cox\ ((2\ ØF + Vsb)^{1/2} - (2\ ØF)^{1/2})$

in which the parameterY, known as the *substrate-bias* (or *body-effect*) coefficient is given by

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_S}}{C_{ox}}.$$

$= (2*1.6*10^{-9}\ 11.7*80854*10^{-14}*10^{14})^{1/2} / 1.7265*10^{-7}$

$= 0.03334$

Where,

$Na = 3*10^{16}$

$Tox = 200*10^{-8}$

$ox = 11.7*8.854*10^{-14}$

$Cox = ox / Tox$

$= 3.9*80854*10^{-14} / 200*10^{-8}$

$= (2*1.6*10^{-9}* 11.7*80854*10^{-14} *3*10^{16})^{1/2} / Cox$

$=0.57$

$ØF= KT/q \ln(NA/ni)$

$= 1.38*10^{-23} *300/1.6*10^{-19} \ln (10^{14} / 1.5*10^{10})$

$=0.228$ V

$Vt = Vt0$

Then, at $V_{sb} = 2.5$ volts

$$V_{T2.5} = V_{T0} + 0.57\left(\sqrt{0.75+2.5} - \sqrt{0.75}\right) = V_{T0} + 0.53$$

As is clear, the threshold voltage increases by almost half a volt for the above process parameters when the source is higher than the substrate by 2.5 volts.

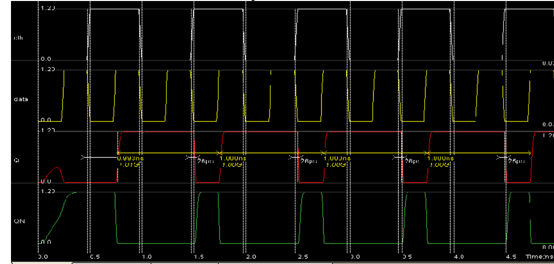

Fig.10. Delay latch with 3 lamda technology output wave

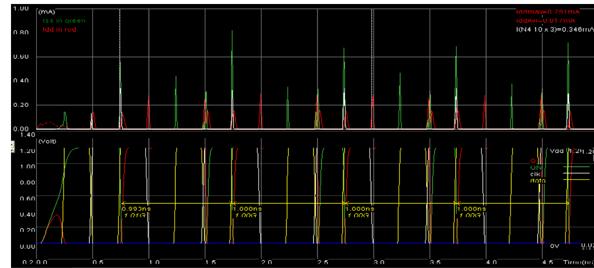

Fig.11. Delay latch with 3 lamda technology output wave

The decrease in device dimensions increases substrate doping densities results in significant increase in horizontal and vertical electrical field in the channel region. Electrons and hole gaining high kinetic energies in the electric field may, however, get injected in in to the gate oxide , and cause permanent changes in the oxide interface charge distribution, degrading the current voltage characteristic of the MOSFET. The channel hot electron effect caused by electron flowing in the channel region , from the source to drain. This affects the transistor characteristic by causing a degradation in transconductance, Vt, Ids capability.

Since the gate length, L, is effectively the base width of the parasitic bipolar transistor, it has a strong effect on the I-V curve. As the ratio of the breakdown voltage to the snapback voltage is 1/n, the current gain of the bipolar transistor raised to some power. The breakdown voltage should be determined only by the drain-substrate junction profile and thus be constant vs. gate length, unless the gate length is so short that punchthrough occurs before avalanche breakdown.

IV. Conclusion

In this paper, we show that short channel effects on the MOSFET characteristics strongly depends on the transistor aspect ratio and in particular on the transistor channel width, so that even digital applications may be strongly disturbed by these effects. In fact, the transconductance and drain saturation current of MOSFETs with 2-nm and 2.5-nm gate oxides may dramatically drop in transistors with very narrow channels after these effects, i.e., MOSFETs largely used for digital circuits. It affects the transistor electrical characteristics to a degree depending on the degradation level and area of the gate oxide broken region. This effect is due to the formation of a localized oxide damaged region likely

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trapping negative charge over a large portion of the channel width, around the SB conductive path, as the damaged oxide region becomes wider due to thermal dissipation and defect generation.

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