International Journal of Electronics Communication and Computer Engineering
Volume 8, Issue 2, ISSN (Online): 2249–071X

Power and Delay Improvement of Edge Triggered Flip Flop Design Using Transmission Gate

Rachit Pawar*
email id: ecengg.rachitpawar@gmail.com

Ashish Raghuwanshi
email id: ashishraghuwanshi.06@gmail.com

*Corresponding author

Date of publication (dd/mm/yyyy): 20/04/2017

***Abstract* — The most of the area in sequential digital integrated circuits is consume by flip flops and most of the power is dissipates due to the dynamic power dissipation by voltage transition at internal nodes of circuit when both input and output node is at the same state. In related work, many power dissipation minimization techniques are use which may cause increase in number of transistors for design. This paper discusses the schematic and CMOS layout design and its timing simulation of edge triggered flip flop with cross connected NAND Logic design by transmission gates. The use of transmission gate exhibits area and power optimized design as the transmission gate (TG) reduces number of stray capacitance and less number of transistors.**

***Keywords* — Flip-Flop (FF), TG, Hold Time, Latch, Performance, Improvement, Process Variations, Setup Time.**

I. INTRODUCTION

The single phase clocking with pass transistor logic is use in synchronized flip flop design. Power dissipation is optimizes without using local clock buffers. Since the data activity becomes low, total power dissipation is drastically reduced. But the use of individual PMOS generates the output logic '0' which is degraded by threshold voltage to pass through a substantially large drain current. It is difficult to overwrite the master latch because PMOS pass-transistors are located in front of the master latch. Latches are not commonly used in digital designs, because of some limitations such as difficult timing analysis and high susceptibility to hold time violations. Hold Time Violation problem of latches is mitigated by reducing the clock duty cycle. This work will try to reduce the transistor size by reducing the coupling without degrading the performance of the MOSFET devices. We will do the parametric analysis on delay, number of transistors and subthreshold power dissipation etc ..

I.1 Timing and delay definitions for flip-flops:

The performance of a flip-flop is qualified by three important timings and delays: propagation delay (Clock-to-Output), setup time and hold time. They reflect in the system level performance of the flip-flops. Setup time and hold time define the relationship between the clock and input data.

- *Propagation delay:*

Propagation delay (Clock-to-Output) is the time delay after arrival of clock's active edge that output is considered stable. Clock-to-Output equals the time it takes for the output to change after the occurrence of the clock edge. Usually propagation delay differs for low-high transitions and high-low transitions. So propagation delay of the flip-flop is by definition maximum value of these two delays.

- *Setup time*

In order to function correctly, the edge-triggered flip-flop requires the input to be stable some time before the clock's active edge. This period is called the setup time of the flip-flop. The data value must remain stable around the time clock signal changes value to ensure that the flip-flop retains the proper value. As setup time may differ for low-high transitions and high-low transitions, setup time is by definition maximum of the values obtained for low-high and high-low transitions

- *Hold time*

Flip-flop design requires the state of the input to be held for some time after the clock edge. The time after the clock edge that the input has to remain stable is called the hold time. Basically hold time can be negative meaning that data can be changed even before clock edge and still previous value will be stored. Hold time is by definition maximum of the values obtained for low-high and high-low transitions.

In these definitions, propagation delay, setup time and hold time are considered as independent variables. However what happens in reality shows that these parameters are not independent from each other. For instance, propagation delay is strongly related to the data arrival time.

II. Failure mechanisms in flip-flops:

This failure appear for edge triggered flip-flops built using a pair of latches driven on opposite clock phases. Consider the model of an edge-triggered flip-flop . Ideally the flip-flop should exhibit the setup and hold times of its master latch with respect to the rising edge of clk, and should cause data to appear on the output with the delay times of the slave latch with respect to the same clk edge. The latch is supposed to hold the value sampled on the rising clock edge until the next rising clock edge. It will do so, however, only if the delay time of the master latch is greater than the hold time of the slave. If this condition is not met, data will race-through to output, changing it on the inactive clock edge. This condition must be guaranteed solely by correct construction of the flip-flop and is independent of external parameters. The flip-flop can fail in a more subtle way. If setup time of the master latch is small and propagation delay of the master latch is large, then the behaviour of the Output may no longer be governed solely by the properties of the slave latch. Data can race through both latches on the active clock edge and may even cause multiple transitions on the Output. This undesirable behaviour of the flip-flop can be avoided by assuming larger setup time for the flip-flop (larger than master latch's setup time), at the cost of increased cycle time.

International Journal of Electronics Communication and Computer Engineering
Volume 8, Issue 2, ISSN (Online): 2249–071X

III. Edge Triggered Master Slave Base Flip Flop Design:

Master–slave FFs are widely used in digital circuits. If we apply the inverted clock signal to the master latch, the FF changes to two similar latches that behave like one. The state of a latch or flip-flop is switched by a change in the control input. This momentary change is called a trigger, and the transition it causes is said to trigger the flip-flop. The D latch with pulses in its control input is essentially a flip-flop that is triggered every time the pulse goes to the logic-1 level. As long as the pulse input remains at this level, any changes in the data input will change the output and the state of the latch.

The behaviour of the master–slave flip-flop just described dictates that (1) the output may change only once, (2) a change in the output is triggered by the negative edge of the clock, and (3) the change may occur only during the clock's negative level. The value that is produced at the output of the flip-flop is the value that was stored in the master stage immediately before the negative edge occurred . It is also possible to design the circuit so that the flip-flop output changes on the positive edge of the clock. This happens in a flip-flop that has an additional inverter between the Clk terminal and the junction between the other inverter and input En of the master latch. Such a flip-flop is triggered with a negative pulse, so that the negative edge of the clock affects the master and the positive edge affects the slave and the output terminal.

III.1 Edge Triggered Toggle Flip Flop Design:

The T (toggle) flip-flop is a complementing flip-flop and can be obtained from a JK flip-flop when inputs J and K are tied together. When T = 0 (J = K = 0), a clock edge does not change the output. When T = 1 (J = K = 1), a clock edge complements the output. The complementing flip-flop is useful for designing binary counters.

The T flip-flop can be constructed with a D flip-flop and an exclusive-OR gate as shown in Fig. (b). The expression for the D input is

$$D = TQn + TnQ$$

When T = 0, D = Q and there is no change in the output. When T = 1, D = Qn and the output complements. The graphic symbol for this flip-flop has a T symbol in the input.

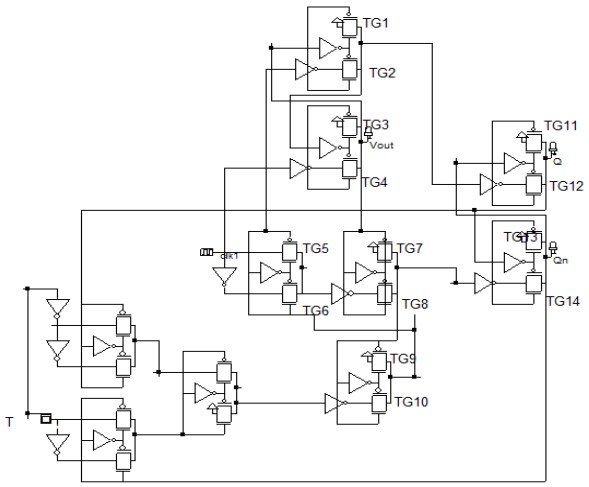

Fig 1: CMOS Schematic Circuit for Toggle Flip-flop.

III.2 Edge Triggered J K Flip-flop Design

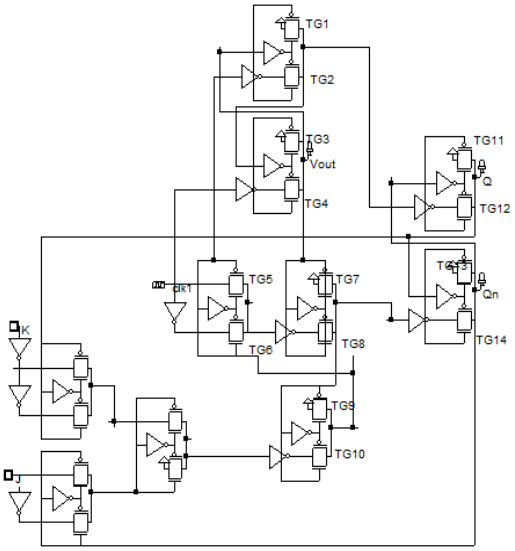

Fig 2: CMOS Schematic Circuit for J K Flip flop.

III.3 Layout Design and Timing Simulation of Edge Triggered Flip Flop:

The circuit diagram of a JK flip-flop constructed with a D flip-flop and gates. The J input sets the flip-flop to 1, the K input resets it to 0, and when both inputs are enabled, the output is complemented. This can be verified by investigating the circuit applied to the D input:

$$D = JQn + KnQ$$

When J = 1 and K = 0, D = Qn + Q = 1, so the next clock edge sets the output to 1. When J = 0 and K = 1, D = 0, so the next clock edge resets the output to 0. When both J = K = 1 and D = Qn, the next clock edge complements the output. When both J = K = 0 and D = Q, the clock edge leaves the output unchanged.

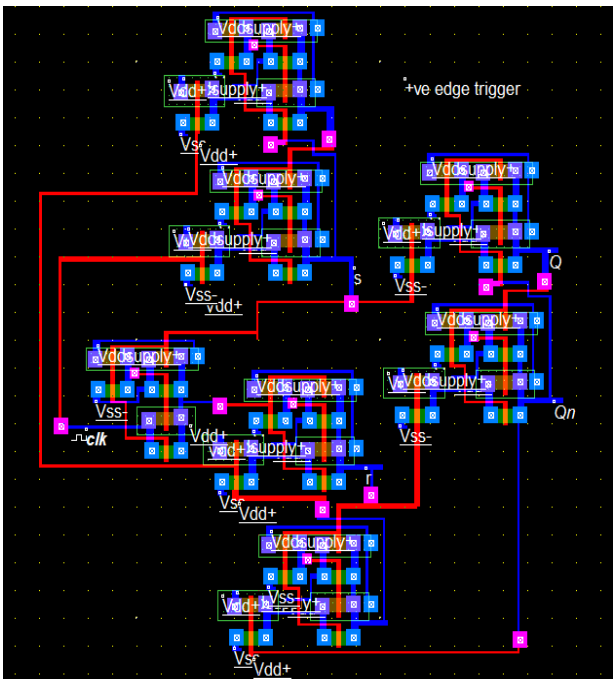

Fig 3: CMOS Layout Design for Toggle Flipflp Design using D Flip flop.

The Fig shows CMOS layout of edge trigger master slave transmission gate base toggle Flip flop design with 3 level trigger TG Latch. The output Qn is connected to input port D. The total number of transistors are consist of 54 transistors. The channel length of both NMOS and PMOS is 0.05um. The channel width is 0.125 um for both NMOS and PMOS transistor. The total channel length area is 2.7um.

Clk	T in	Q Out	No. of T	Ouput Load	Power Dissipation	Delay
0-1	X	No Change	54	0.57 fF	0.6uW	0.007ns
1-0	0	1				
1-0	1	0				

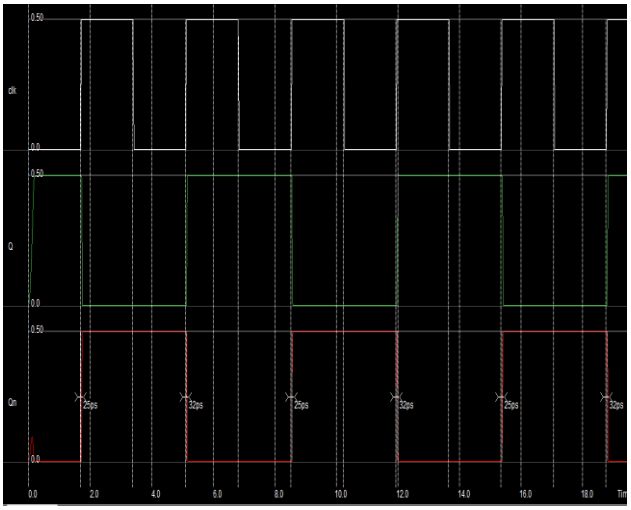

Fig 4: Timing Simulation of Toggle Flipflp Design using D Flip flop.

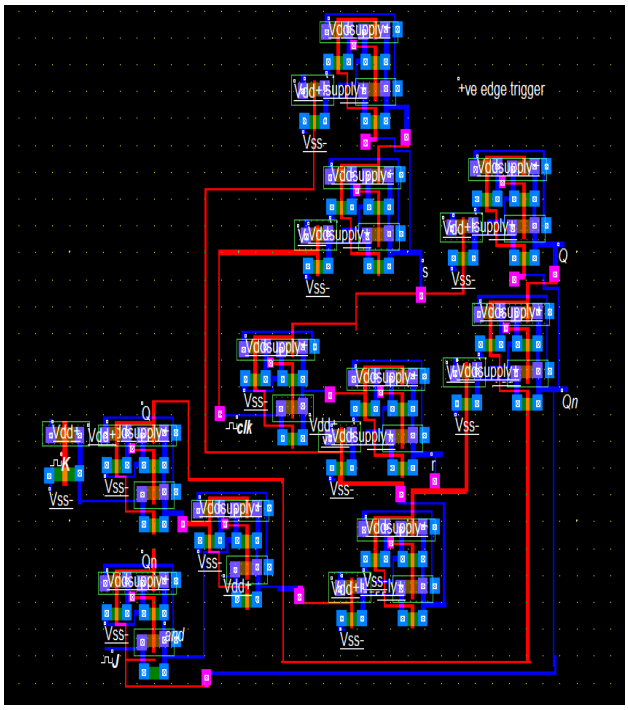

Fig 5: CMOS Layout Design for J K Flip flop using D Flip Flop

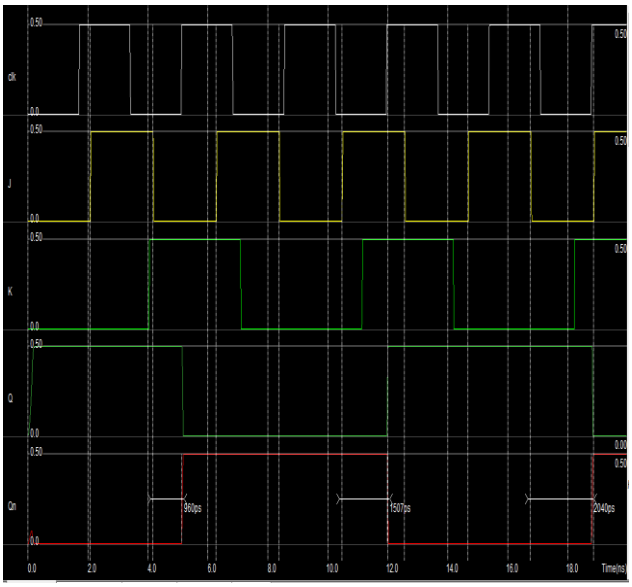

Fig 6: Timing Simulation of for J K Flip flop using D Flip flop

Fig 6 shows tie timing simulation of J K Flip flop design by characteristic equation and by using D Flip flop.

The fig 5 shows CMOS layout of edge trigger master slave transmission gate base J k Flip flop design with 3 level trigger TG Latch. The Flip flop is design with characteristic equation of JK Flip flop and by using CMOS layout of D Flip flop. The total number of transistors are consist of 72 transistors. The channel length of both NMOS and PMOS is 0.05um. The channel width is 0.125 um for both NMOS and PMOS transistor. The total channel length area is 3.6um.

Clk	J input	K input	Q Out	No. of T	Output Load	Power Dissipation	Delay
0-1		X	No Change	72	0.69fF	0.8uW	0.008ns
1-0	0	0	0				
1-0	0	1	1				
1-0	1	0					
1-0	1	1					

III. CONCLUSION

This paper discusses the schematic structure and its working for edge triggered flip-flops design using three cross connected latch and its timing simulation. The schematic and its CMOS layout is design using transmission gate which exhibit the best power and delay performance trade-off. AS transmission gate are design with less number of stray capacitance and less number of transistors. Design reduces the transistor size by mitigating the problems of short channel without affecting the performance of the CMOS devices. Timing Simulation shows parametric analysis on delay , number of transistors and subthreshold power dissipation. The goal is to trade off between these limitations and thus propose design which reduces both leakage and dynamic power with minimum possible area and delay trade off.

REFERENCE

[1] Mehrzad Nejat, Bijan Alizadeh, and Ali Afzali-Kusha "Dynamic Flip-Flop Conversion: A Time-Borrowing Method for Performance Improvement of Low-Power Digital Circuits Prone to Variations" IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 23, No. 11, November 2015 pp no. 2724-2727.

[2] K. Kobayashi, K. Kubota, M. Masuda, Y. Manzawa, J. Furuta, S. Kanda, and H. Onoder "A Low-Power and Area-Efficient Radiation-Hard Redundant Flip-Flop, DICE ACFF, in a 65 nm Thin-BOX FD-SOI" IEEE Transactions On Nuclear Science, Vol. 61, No. 4, August 2014 pp no. 1881.

[3] A.Parvathi karthica "Power Efficient Synchronous Counter Using Transmission-Gate Based Master-Slave Flip-Flop With Modified Logical Effort Optimization" International Conference on Electronics and Communication Engineering (ECE) 7th April 2013, Bangalore pp no./ 86.

[4] David J. Rennie, and Manoj Sachdev "Novel Soft Error Robust Flip-Flops in 65nm CMOS" IEEE Transactions On Nuclear Science, Vol. 58, No. 5, October 2011 pp no 2476.

[5] David Rennie, DavidLi, Manoj Sachdev, Bharat L. Bhuva, Srikanth Jagannathan, ShiJieWen, and Richard Wong "Performance, Metastability, and Soft-Error Robustness Trade-offs for Flip-Flops in 40 nm CMOS" IEEE Transactions On Circuits And Systems—I: Regular Papers, Vol. 59, No. 8, August 2012 pp no. 1626.