Reduction of Static Power Leakage in CMOS VLSI Circuits

Shailesh M. Keshkamat

Abstract — As CMOS IC Technology is scaled down to lesser dimensions low power becomes a significant parameter of consideration in system design due to Static Power Dissipation occurring in standby mode. This paper reports the design and implementation of logic circuits for reduction of leakage power in device with channel length scaling to sub-100nm. A circuit technique to mitigate the leakage currents in MOSFET through controlling the voltage at the source terminal is implemented and the power dissipation results are compared with that for conventional technique. This has been carried out on the universal gates for the design of combinational and sequential circuits. Improvements in the power dissipation have been observed through the simulation results obtained using Cadence Virtuoso at 45nm technology.

Keywords — Static Power Dissipation, Sub-100 Nm, Source Terminal, Universal Gates.

I. INTRODUCTION

The Integrated Circuit (IC) invented nearly four decades ago is undergoing continuous reduction in size while improving performance parameters like speed of operation and reduces size. To achieve these criteria scaling techniques have evolved. With the evolution of VLSI technology, IC Performance has been increased drastically but, while designing such circuits, challenges viz. reverse bias leakage, Sub threshold leakage, Gate Oxide tunneling current, Gate Induced Drain Leakage (GIDL) etc. have to be overcome [1], [2].

The subthreshold leakage current is the most predominant amongst all the leakage current sources and it becomes extremely challenging for research in current and future silicon technologies.

II. STATIC POWER DISSIPATION

For the CMOS inverter equivalent circuit shown in Fig. 1, if input = '0', the associated n-device is OFF and the p-device is ON. The output voltage is 'Vdd' or logic '1'. When the input = '1', the associated n-device is ON and the p-device turns OFF. The output voltage is logic '0' or 'Vss'. It is evident that one of the 2 transistors is always OFF during either of the logic states. Since no current flows into the gate terminal, and there is no current path from Vdd to Vss, the resultant quiescent (steady-state) current, and hence power 'Ps', is zero. However, there is some small static dissipation due to reverse bias leakage between diffusion regions and the substrate. In addition, subthreshold conduction can contribute to the static dissipation. The drain-source current of a transistor operating in the weak inversion region is known as subthreshold leakage current [3], [4]. The diffusion current of the minority carriers in the channel for a MOS device causes the sub threshold leakage current.

III. LEAKAGE CURRENT REDUCTION TECHNIQUES

This section describes few techniques used to reduce power dissipation in CMOS circuits. The MT CMOS Power Gating Technique [5], [6] shown in Fig. 2 introduces a SLEEP transistor by inserting high threshold devices in series with low threshold transistors between the power supply and ground. In this technique the sleep transistors are turned OFF thereby shutting down the power supply to the circuit creating virtual supply and ground rails.

In the LECTOR [7], [8] technique shown in Fig. 3 below, two leakage control transistors (PMOS and NMOS) are introduced between the pull-up network and pull-down network.

These transistors are connected as such that one of the transistors is always near the cut-off voltage for any input combination hence increasing the path resistance from leakage currents.
IV. METHODOLOGY

This section describes the method used to reduce static power dissipation in CMOS VLSI Circuits. Here both the conventional and modified circuit diagrams are described to compare power dissipation for NOT gate, using 45 nm technology. The simulation for transient and DC conditions is done using CADENCE Virtuoso [9], [10] simulation.

As evident from Fig. 6(a) and 6(b) the DC analysis is identical to both the techniques which means that the logic operation of gate remains unchanged in spite of 2 additional transistors being included in the circuit layout. Also from Fig 7(a) and 7(b) the difference in power dissipation is clearly visible indicating drastic reduction of static power for both logic ‘0’ and logic ‘1’ conditions.

For the Logic ‘0’ state the conventional NOT gate has dissipation of 75 pW whereas for proposed technique the dissipation is approximately 15 pW. Likewise for the Logic ‘1’ state the conventional NOT gate dissipates approximately 15 pW power while in the proposed method the power drastically reduces to 5 pW.

The comparison of power dissipation for NOT gate for the aforementioned techniques is given in Fig. 8.
V. RESULTS FOR OTHER GATES/CIRCUITS

The above mentioned technique was successfully applied for other gates viz. NAND, NOT and also other combinational and sequential circuits. Table II below gives comparison of overall power dissipation for such circuits. From the results shown in Table II below it is clearly evident that the power dissipation using proposed technique got reduced to large extent with an increase of complexity of the digital circuit. Design trade – off has to be done here since there is obviously an increase of area of the circuit due to increase in number of transistors.

Table II. Power dissipation results for various digital circuits.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Power dissipation, pW</th>
<th>% change</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Conventional</td>
<td>Proposed</td>
<td></td>
</tr>
<tr>
<td>NOT</td>
<td>44.024</td>
<td>8.06</td>
<td>4.46</td>
</tr>
<tr>
<td>NOR</td>
<td>16.55</td>
<td>12.5</td>
<td>0.32</td>
</tr>
<tr>
<td>D latch (using NAND)</td>
<td>3.39</td>
<td>0.16</td>
<td>19.03</td>
</tr>
<tr>
<td>SIPO Shift register</td>
<td>16033.8</td>
<td>631.95</td>
<td>24.37</td>
</tr>
</tbody>
</table>

VI. CONCLUSION

Power dissipation is unavoidable especially as technology scales down. Techniques must be devised to reduce power dissipation. A low leakage power circuit technique that controls the source voltage of the MOSFET through the leakage currents of another MOSFET is successfully implemented. Maximum improvement in the power dissipation depends upon the amount of leakage currents that are supplied to the source terminal of the subjected MOSFETs. Hence the proposed technique provides the better results compared to conventional technique. The technique can be implemented for larger and complex digital circuits using either NAND realisation or NOR only realization for digital equivalence.

REFERENCES


AUTHOR’S PROFILE

Shailesh M. Keshkamat born in Belgaum, Karnataka – INDIA, in the year 1978, has obtained degree of B. E. in Electrical and Electronics Engineering from and M. Tech. in VLSI Design and Embedded Systems from KLE’s College of Engineering and Technology, Belgaum – Karnataka, in the year 2006. He has teaching experience of 16 years, with the career starting as LECTURER, and currently working as ASSISTANT PROFESSOR in Department of Electronics and Communication Engineering, Gogte Institute of Technology, Belgaum – Karnataka. His field of interest include design, analysis, characterization and modeling of Low power VLSI Circuits, optimization for small geometry devices, and characterization of Mesa Isolated narrow width MOSFET. Prof. Keshkamat is Life Member of ISTE and Student Member of IEEE.