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Low Power Low Voltage OTA using Adaptive Bias

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***Abstract* – The very fast growing market of portable equipment is increasing interest in low power integrates circuit. So, designing low power integrated circuits requires reduction of supply voltages and interconnection parasitic to minimum but reduction in supply voltage implies series of problems in circuit design. To overcome these issues, an Ultra low power low voltage two stage class AB CMOS fully differential operational amplifier Op-Amp) operating at 0.4 V supply design in low cost 90nm CMOS technology is proposed.**

***Keywords* – Class AB, CMOS, Op-Amp.**

I. INTRODUCTION

The increasing demand for long-life battery operated portable equipment is moving the current trend toward low power design [1]. Portable battery powered equipment requires less power to ensure an active period of operation from a battery and systems need to have very long life of battery since most of the times it is impossible to replace or recharge batteries that's why the less supply voltage is essential.

In Analog circuits, transistors operating in the weak inversion region consume minimum power for an acceptable operation and power dissipation is less but operates more slowly. So the operation in the weak inversion region is more helpful for energy constrained applications where saving energy is the primary goal, while sometimes we need to scarify the speed [1].

Operational amplifiers are essential block in the modern integrated systems. They are used in wide variety of circuit topologies such as data converters, filters and voltage regulators [2]. In old technologies, schematic with a high supply voltage achieves high gain, wide bandwidth and good slew rate while in the modern technologies means for short channel length, the design of an op amp with good performances is very difficult because of the intrinsic limitations of the transistor's analog performances.

To address the above, this paper presents a CMOS fully differential operational amplifier focusing ultra low-power applications. The main features are: sub-threshold operation, ultra low-power consumption, class AB operation and enhance slew-rate.

The effective implementation of any system needs deep study and analysis of various papers related to the topic. So, literature survey for low voltage low power operational amplifier is as follows:

To process the signals with the maximum signal voltage at a certain supply voltage requires rail to rail input stages. So, rail to rail input stage means circuit has to work perfectly at any common mode input voltage [4]. As it is well-known, the PMOS and NMOS transistor pair is ON for low and high common-mode input voltages respectively. By placing an nchannel and a p-channel input pair in parallel, rail to rail extension of common mode input range can be achieved [1].

Low voltage power efficient operation and high slew rate is difficult with input stage of conventional class A op amp since the bias current limits maximum output current. So it leads to more difficult in sub-threshold operation were bias currents are quite smaller. To overcome this issue, adaptive bias circuits can be used. So when large differential input signal detects then adaptive bias circuit automatically boost dynamic currents and provides maximum current levels above the quiescent currents. To reduce static power dissipation these currents can be made very low [1].

As in every fully differential operational amplifier high CMRR is required to reject common input signals. To achieve this, Common mode feedback or common mode feed forward circuits can use. So, in order to kept DC voltage gain constant in spite of variations in common mode input voltage, CMFF circuit also biases output stage [1].

There are various frequency compensation techniques such as miller and cascade compensation are used to design the stable two stage op amps, drawbacks of miller compensation technique are low speed and power supply rejection ratio (PSRR) as compared to cascade. In case of cascade compensation technique, achieves low power consumption, high speed and high PSRR at the expense of complex analysis procedure and design [2].

For reducing power dissipation most of the low power op amp works in the weak inversion mode. Due to technology improvement, it is desired to reduce power supply to minimize power dissipation due to this many challenges face the analog designer. As the power supply voltages begin to approach 2V, op amp topology like folded cascade should be used. For low voltage low power operation folded cascade is a good solution as it provides large ICMR and better frequency performance which is required for low voltage operation and can be designed for low power operation also [3].

Conventional output stages have an efficient class AB biasing but provides short rail to rail voltage range because their output transistors are connected in common drain

configuration. To overcome this issue output transistor in a rail to rail output stages must be connected in a classical common source configuration [4].

The normal two stage op-amp has large output swing but needs gain boosting in the first stage for high gain and a lot of current in the second stage to get large unit gain bandwidth which make it complex and not entirely suitable for low power designs. Then a novel low power two stage op amp is proposed, which makes use of one simple class AB architecture, not gain boosting, in the first stage for high gain and another class AB architecture for large output swing in the second stage [5].

In the past, circuits have one input and one output with respect to ground, But Low power supply makes single ended circuits are very difficult to perform optimally. So, alternative to single-ended circuits is fully differential circuit which is used to double the output swing. In fully differential circuits output terminals are equal but opposite polarity. Additionally fully differential circuit improves output swing, common mode rejection ratio and linearity [6]. This paper is organized as follows: Section II describes the proposed op amp, while Section III reports the results obtained for 90nm CMOS implementation. Conclusions are drawn in Section IV.

II. Description of an Amplifier

The Operational amplifier is made up of different stages and the working principal of each stage is described in this section. The idea behind the proposed fully differential operational amplifier is shown in Fig.1. It can be divided into two main parts: first one is the core of the amplifier composed by a rail to rail input stage using complementary input pairs with adaptive biased and the output stage of class AB, second stage is the common mode feed forward circuits (CMFF).

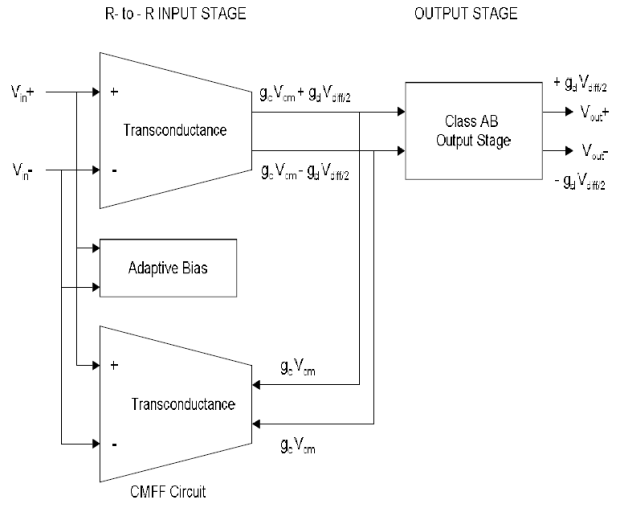

Fig.1. Conceptual schematic of the proposed operational amplifier [1]

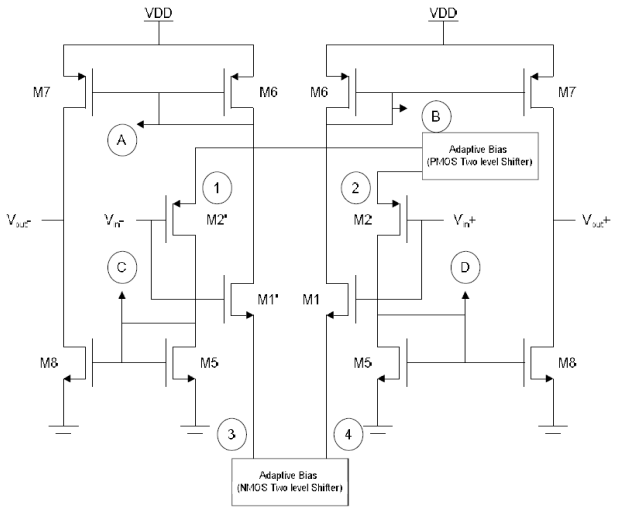

Fig.2. (a) Core of the proposed operational amplifier with adaptive bias.

Fig.2 (a) shows the core of the proposed operational amplifier with adaptive bias and detailed description of each part of the fully differential op amp is as follows:

A. Rail to Rail Input Stage

In this Operational amplifier shown in the Fig.2 (a), both NMOS and PMOS input transistors i.e M1 (M1 and M1') and M2 (M2 and M2') respectively operates in sub-threshold region for low voltage, power efficient operation. To reach the negative supply rail, P- channel transistor must be used while holding their drain voltages close to ground and for the positive supply rail, N- channel transistor must be used while holding their drain voltages close to supply voltage. Hence for achieving full rail to rail range P-type and N-type input transistor need to add and processed in a way that trans conductance becomes constant over full rail to rail range. So these are the requirements need to satisfy to design rail to rail input stage [8].

B. Class AB Output Stage

The output transistor M7 and M8 are connected in a classical common source configuration for ensuring the maximum output range and all the transistors i.e M5, M6, M7, M8 operates in sub-threshold region. The conventional class A before class AB in which device amplifies the complete input cycle. So when there is a no signal is applied the amplifier remains active and dissipate more leakage power. Therefore class A is very inefficient but gives less distortion. In case of class B device amplifies half input cycle and for other half device gets off hence power dissipation in class B is less than class A but high distortion. In class AB Operation device operates same as that of class B for half waveform but also conducts a less amount on the other half. Hence region where both devices simultaneously are nearly off is reduced. Therefore Class AB is a trade-off between class A and Class B and widely used in output stage of operational amplifier [9].

C. Adaptive Bias Circuit

The maximum current delivered to the load is B.Ibias and slew rate is therefore B.Ibias/CL Where, B is output current mirror ratio and CL is load capacitance. To avoid the limitations of settling time by slew rate, B and/or Ibias should be large. An increase in the Ibias leads to the same increase in the static power dissipation and larger B values not only increase slew rate but also gain bandwidth product and current efficiency. So, it suggest that B should be maximized but unfortunately, assuming operation in strong inversion of the current mirrors, static power consumption is IQ = SR.CL(1+1/B), even for very large B slew can only increase proportionally to static power consumption. Therefore it is difficult to achieve high slew rate with low static power consumption using a Conventional class 'A' op amp topology. To overcome these issue adaptive bias circuits can be used [10].

The PMOS and NMOS Two level shifter circuits are shown bin the Fig.2 (b) and (c) respectively. An adaptive biasing technique is used to achieve class AB operation and slew rate enhancement [10]. Transistors M9-M12 operates in subthreshold region and M3-M4 operate in the strong inversion region. Both NMOS and PMOS input transistors operate in sub-threshold are cross coupled by two level shifter. Very low output impedance DC level shifters are required in order to drive the low impedance source terminals of both transistors in pair. The dc level shifters must also be able to source large currents when the circuit is charging or discharging a large load capacitance [10].

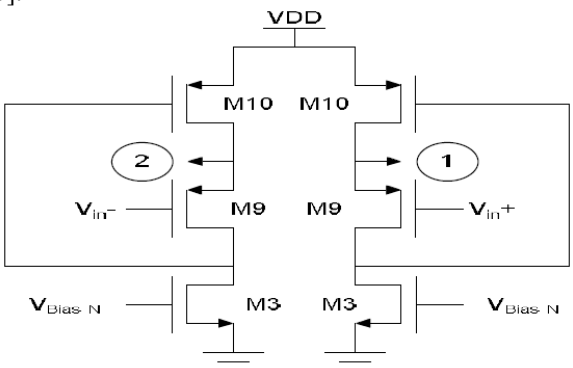

Fig.2. (b) PMOS Two Level Shifter.

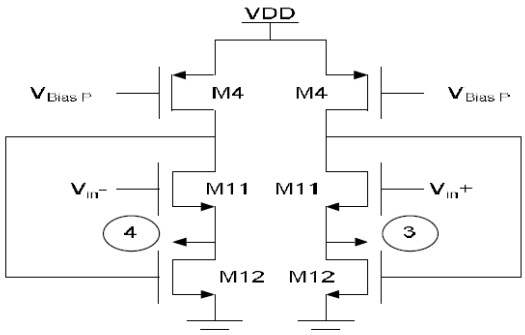

Fig.2. (c) NMOS Two Level Shifter

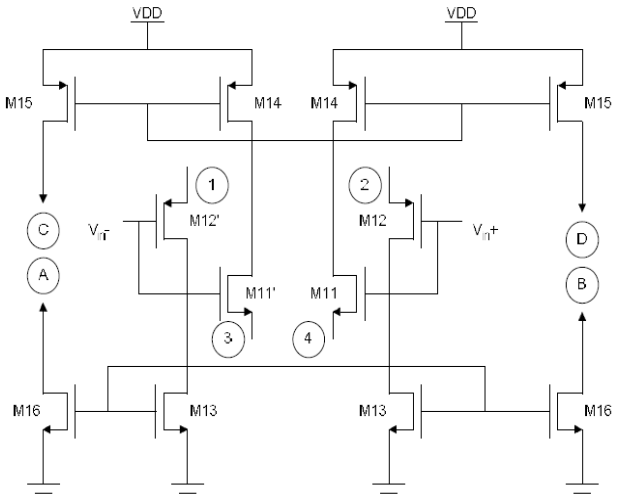

Fig.3. CMFF Circuit

Transistors M11-14 and M12-13 generate currents which are added to the core of op amp by means of transistors M15 and M16 respectively and all transistors are operate in subthreshold region [1].

III. Performance of an Amplifier

The performance of the proposed op amp are summarized in table 1, in which we also make a comparison between our design and other previous fully differential op amp designs [1,11-13]. This comparison shows that the performance of the proposed op amp is better than the earlier op amps. The simulations which we will take as a primary results from the circuit in which adaptive biasing technique such as Winner Take all (WTA) is used shown in Fig.4,5,6,7,8 and 9. In WTA both the NMOS and PMOS input transistor operate in the subthreshold region are not cross coupled and that differentiates WTA from Two Level shifter. So, Fig.4 shows open loop DC gain of 44.24 dB and Unity gain frequency of 25.11 MHz whereas CMRR(46.7 dB), Phase margin(26.4 dB), slew rate (4.7 V/µs), output swing (320 mV) and Power consumption (4.8 µW) are shown in Fig 5,6,7,8 and 9 respectively. The proposed op amp is being designed in a low cost 90 nm CMOS technology with 0.4 V supply voltage. Simulations are being done using spectre with a BSIM3v3.2 model for the UMC 90 nm CMOS technology. The expected results of op amp are as follows: The open loop DC gain will be more than 50 dB, while unity gain frequency will be more than 40 kHz with CMRR and Phase margin will be more than 65 dB and 65o respectively, the power consumption of operational amplifier will be less than 4µW, the slew rate will be more than 0.10 V/µs in a voltage follower configuration with the same CL = 10 pF connected to each output.

Table1. Comparison between fully differential op amp performances

Parameter	[1]	[11]	[12]	[13]	This work
Supply Voltage	0.8 V	0.5 V	0.8 V	0.8 V	0.4 V
Technology (CMOS)	0.18 µm	0.18 µm	0.18 µm	0.35 µm	0.09 µm
DC Gain	51 dB	55 dB	68 dB	66 dB	>50 dB
Unity gain frequency	40 kHz (CL = 10pF)	8.72 MHz (CL = 10pF)	8.12 MHz (CL = 10pF)	3.4 MHz (CL = 10pF)	>40 kHz (CL = 10pF)
CMRR	65 dB	78 dB	N/A	N/A	>65 dB
Phase margin	65^0	61^0	89^0	80^0	$>65^0$
Slew Rate	0.12 V/µs	1.35 V/µs	2.89 V/µs	4.7 V/µs	>0.10 V/µs
Input swing	Rail-to Rail	N/A	Rail-to Rail	Rail-to Rail	Rail-to Rail
Output swing	744 mV	N/A	700 mV	500 mV	>300 mV
Power	1 µw	77 µw	94 µW	194µW	<4 µW

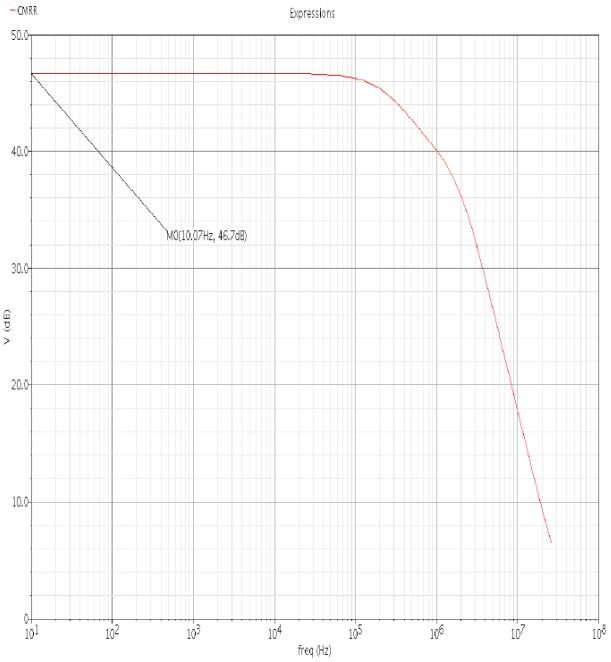

Fig.5. CMRR of an Op amp

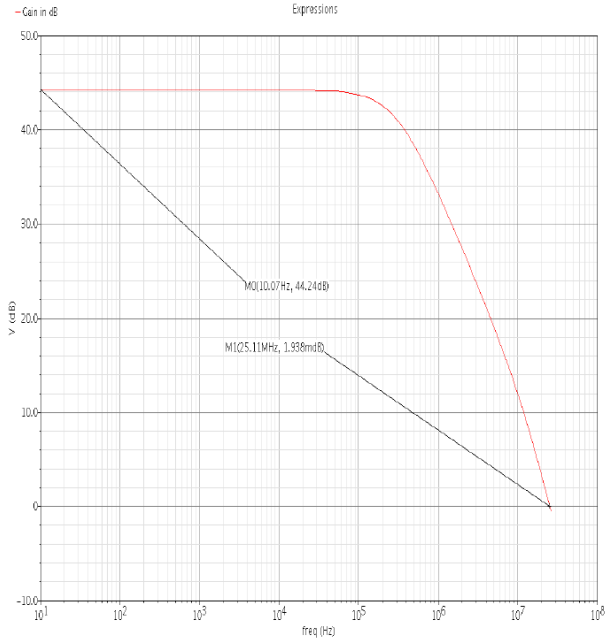

Fig.4 Gain Vs Frequency Plot

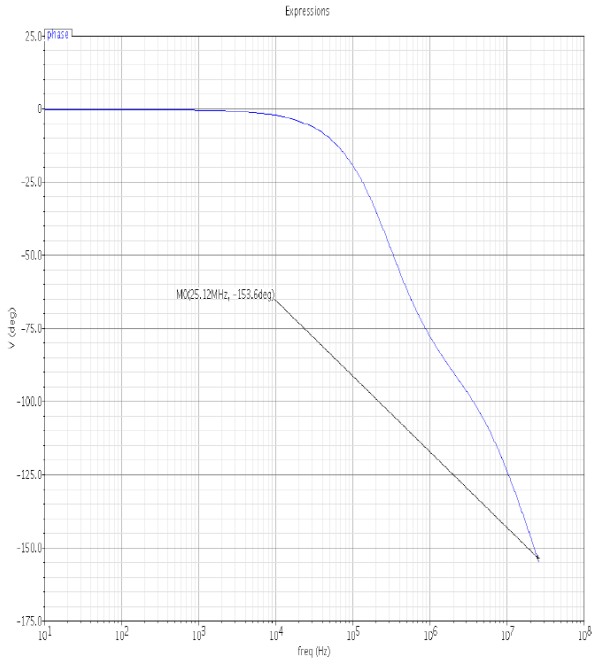

Fig.6. Phase Vs Frequency plot

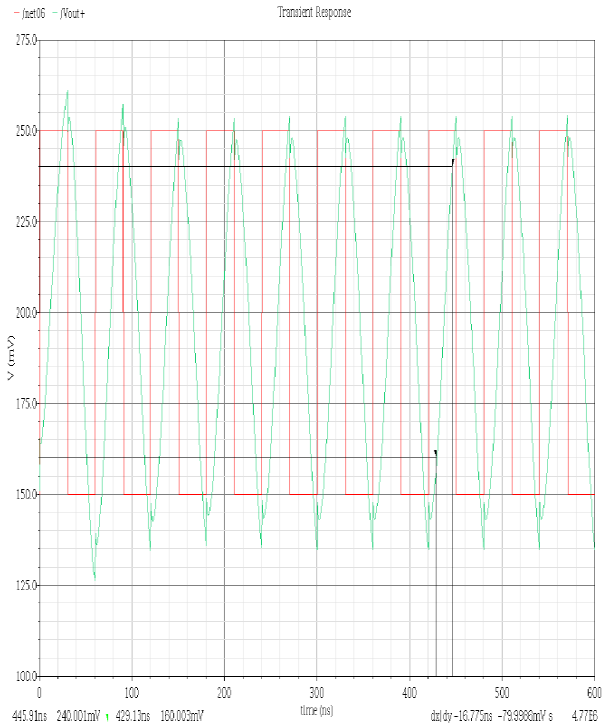

Fig.7 Slew rate of an Op amp

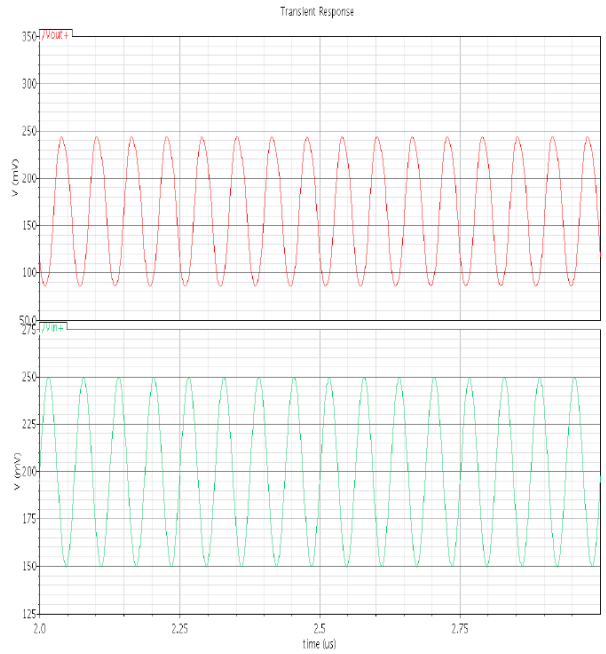

Fig.8. Transient Response of an Op amp

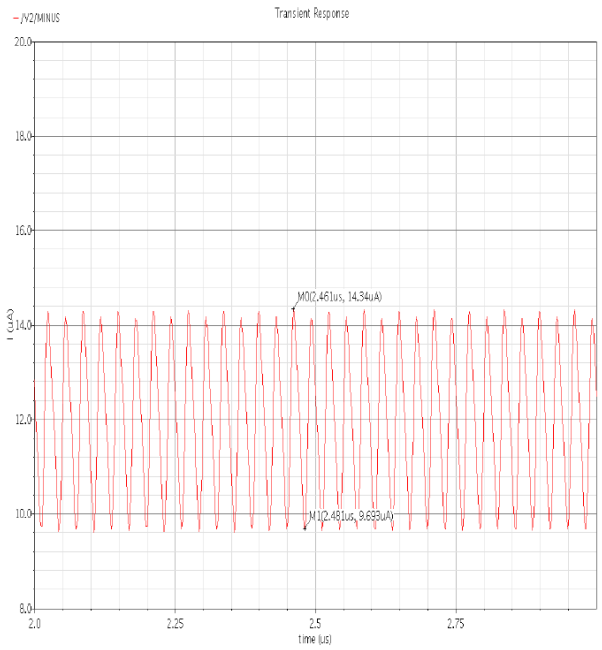

Fig.9. Total DC Current of an Op amp

IV. CONCLUSION

By observing the present day increasing demand for the portable battery powered equipment, a simple and area efficient low power low voltage fully differential operational amplifier is proposed. The expected results shows proposed op amp is very efficient than earlier op amps and it could have wide application range in analog circuit where operations are carried out with very low power supply. Proposed operational amplifier working at very low supply voltage increases battery lifetimes and decreases number of batteries required by the system for active operation while reduction in the CMOS technology to 90 nm consumes less area and make system portable.

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