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Design, Implementation and Analysis of 10bit, 80MS/s Pipeline ADC Using OPAMP Sharing Technique in Cadence Tool

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***Abstract* – In this paper, A 10 bit, 80 MS/s pipeline ADC is design using opamp sharing technique. The opamp is shared between all the consecutive pipeline stages, so that power consumption and die area can minimize. The A/D is designed, implemented and analysed in standard gpdk 180 nm technology library using cadence tool. This converter achieves 68 dB spurious free dynamic range, 59 dB signal-to-noise-plus-distortion ratio,9.58 effective number of bits for a 90 MHz input at full sampling rate, and consumes 30 mW from a 1.8 V supply.**

***Keywords* – Pipeline ADC, Resolution, Low Power Consumption, OPAMP Sharing, Cadence.**

I. INTRODUCTION

With the rapid growth of modern communications and signal processing systems, hand-held wireless computers and consumer electronics are becoming increasingly popular. Mixed signal integrated circuits have a tendency in the design of system-on-chip (SOC) in recent years. SOC designs have made possible substantial cost and form factor reductions, in part since they integrate crucial analog interface circuits, such as ADCs with digital computing and signal processing circuits on the same die [1].

Analog to digital converter are important components in application requiring the interface between analog and digital domain. These are varied and numerous and range from digital radio systems to military and medical sensors to wire-line and wireless communication. High performance application such as broadband communication system require high performance analog-to-digital converters (ADCs) with high resolution and bandwidth. Such application are often the domain of pipeline ADCs, due to their highly efficient and conversion-speed centric architecture. Pipeline ADCs Architecture becomes more and more attractive because it can operate at high sampling rates with high efficiency in terms of power and chip area.

The ADC presented in this paper offers an 8-bit resolution and the sampling rate of 75 MHz. It is implemented in a2.8-bit-per-stage pipelined architecture. By switching off the second stage of the two-stage opamps in the sample-and-hold amplifier(SHA) and subsequent pipelined stages during one of two non-overlapping phases, the power consumption can be significantly reduce.

Section II reviews the conventional pipelined ADC architecture. Section III describes power reduction techniques such as an opamp sharing technique. Section IV describes proposed opamp sharing technique and also described the overall architecture. The measurement results are shown in

Section V and conclusions are drawn in Section VI.

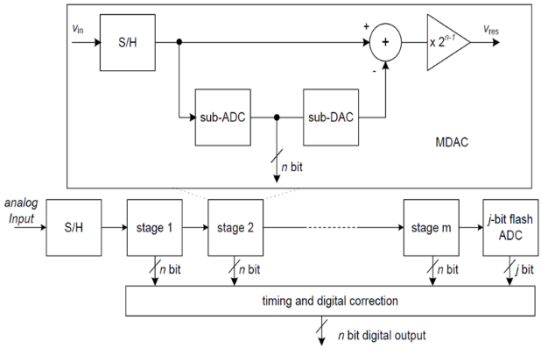

Fig.1. Pipeline ADC Architecture

II. PIPELINE ADC ARCHITECTURE

A typical pipelined architecture uses a number of similar pipelined stages labelled Stage 1, Stage 2, etc., as shown in Fig.1. All of the pipelined stages are similar in construction, consisting of a SHA, a digital-to-analog-sub converter (DASC), an analog-to-digital-sub converter (ADSC), a subtracter, and a multiply by amplifier. The symbol denotes the numberof bits the stage of the pipeline resolves.

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The input is first sampled-and-hold and then digitizedby the ADSC to arrive at the first most significant bits (MSB's), represented by . This digital code is applied tothe DASC to produce an analog

voltage which is subtractedfrom the sampled-and-hold input. The difference represents the residue and is amplified by to scale it back to the fullscale. This amplified residue, is passed to Stage 2 as an input. After performing a similar set of operations as described for Stage 1, Stage 2 resolves the next MSB's. In a typicalimplementation, the stage gain is reduced by a factor of twoand the digital codes , , , etc., are overlapped by 1 bit to perform digital error correction [2].

In this manner, as the input signal is processed by Stage 1,Stage 2 concurrently processes the residue signal fromthe previous sample. The concurrency of operation by eachstage in the pipeline allows the pipelined ADC to achieve high throughput suitable for video applications [2], [3].

In a pipelined architecture, the growth of the hardware is linear with the number of bits resolved. This linear dependence is in contrast with an exponential dependence for a flash architecture. However, a pipelined ADC typically needs high performance analog components such as op-amps to perform the functions indicated in Fig. 1. These high-performance components can consume large amounts of power. In the following sections, a set of power minimization techniques is described for the pipelined ADC's.

III. OPAMP SHARING TECHNIQUE

In OPAMP sharing pipeline ADC, OPAMP is not utilised during the sampling phase and output are reset to common mode. Since consecutive MDAC stages in the pipeline operate in alternate phases, the opamp-sharing technique, illustrated in

Fig. 2, which can be applied to achieve significant reduction in power consumption. In clock phase , MDAC1 is in the hold(or amplification) mode and the shared OPAMP provides the necessary amplification based on the input previously sampled on and . MDAC2, which operates in the alternatephase, is in the sampling mode and the output of the OPAMP issampled on and . In clock phase , MDAC1 is in thesampling mode allowing for the shared OPAMP to be used in MDAC2 for amplification. With this approach, opamp-sharing doubles the utilization of every OPAMP, reducing the total number of OPAMP's required to implement a pipeline A/D, consequently providing significant power and area reductions. We can achieve power reduction by sharing an amplifier between successive stages in a pipeline ADC [4]. However, the amplifier sharing technique has two drawbacks [5]. First, the additional switches that are used to implement this technique introduce series resistance, which in combination with the amplifier's input capacitance affects the settling behaviour of the stage. For higher conversion speeds, the switch resistance can be reduced by using larger switches at the expense of a potential increase in offset voltage due to charge injection and clock feed-through. Second, the non-zero input voltage of the amplifier is never reset. Thus, every input sample is affected by the finite-gain error component from the previous sample. Also, error voltages, including flicker ( ) noise and theOPAMPs intrinsic offset voltage, cannot be cancelled becausethe amplifier is always in the active mode. This shortcoming results in memory effects. At the end of an amplification phase, a potential difference exists between the OPAMP's input s. Aportion of this potential difference is due to the finite open loop gain and bandwidth of the OPAMP and it is input signal dependent. OPAMP with dual inputs have been shown to eliminate memory effects [6], [7]. In this OPAMP, one input pair is utilised for the amplification and other input pair are reset to common mode to common-mode avoiding memory effects. However, to reduce power from opamp-sharing the two input must not be turned on simultaneously.

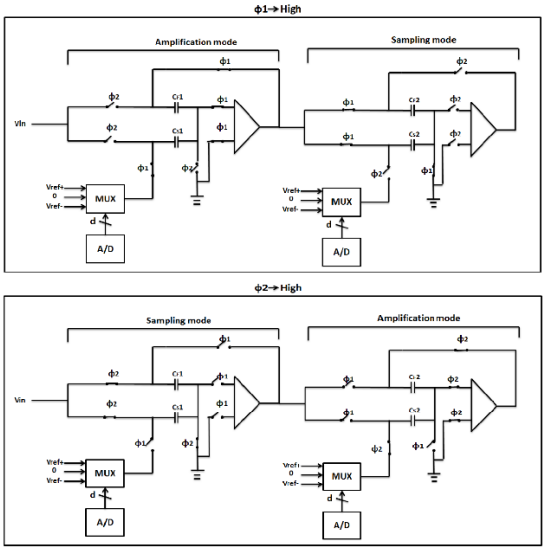

Fig.2. OPAMP Sharing Pipeline A/D

IV. PROPOSED OPAMP

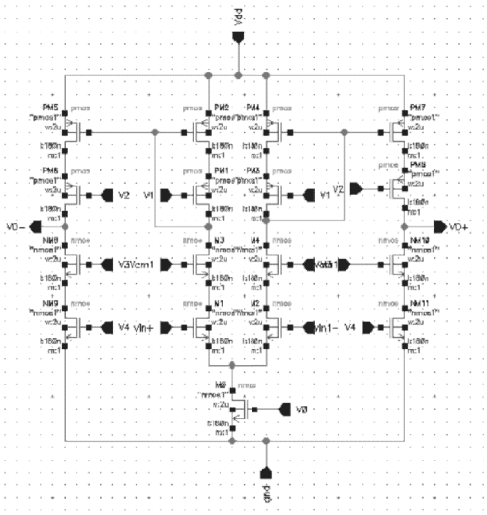

Fig.3. Proposed OPAMP

The schematic of the first and the second stages of the proposed opamp is shown in fig.3. The OPAMP comprises of nmos transistor $M_0 - M_4$ and a switch S_1. In clock phaseΦ_1, the switch $S_1$is open and selecting $M_1$and M_2as theOPAMP input differential pair. The gates of $M_3$and M_4arebiased to $V_{CM_2}$and they serve as cascode transistors to theinput pair. In the next clock phase Φ_2, $S_1$is closed shortingthe drains of $M_1$and $M_2$and selecting M_3M_4as the inputdifferential pair. The gates of $M_1$and $M_2$are biased to $V_{CM_1}$and they operate as cascode transistors for the tail currentsource M_0.

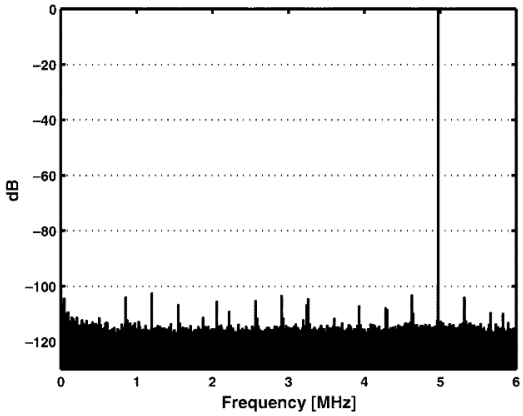

Fig.4. Measured output spectrum

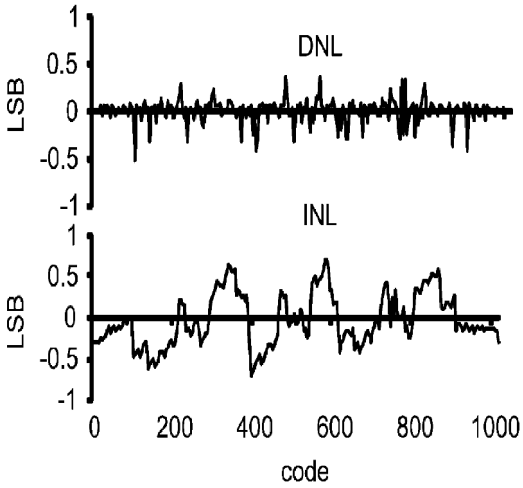

Fig.5. Measured INL and DNL

V. Measurement Result

The 10-bit 80 MS/s pipeline ADC is designed in a 0.18μm CMOS process, Fig. 4 shows the FFT of the ADC outputwhen sampling a 5.023 MHz full-scale sinusoidal input at 80MS/s, and achieves an SFDR of 68 dB, an SNR of 60 dB,and SNDR of 59 dB. The measurement result of proposed A/D are summarised and compared with prior work in Table I. The total power dissipation is 30 mW. The worst case DNL and INL are -0.5/+0.14 LSB and -0.43/+0.4 LSB, as shown in fig.5, respectively.

VI. Conclusion

A operational amplifier (opamp) with dual nmos differential inputs structure which alleviates memory effect and reduces the power consumption is presented. Using this architecture a10-bit, 80 MS/s, 0.18 µm CMOS pipeline ADC that consumes only 30 mW, while achieving an SNDR of 59 dB is achieved. The design merges the front-end SHA into the first MDAC and minimize the size of the sampling capacitance in addition to sharing the opamps in order to achieve the low power consumption.

References

[1] S.Padoan, A.Boni, C.Morandi, F Venturi, “A novel coding schemes for the ROM of parallel ADCs, featuring reduced conversion noise in the case of single bubbles in the thermometer code,”IEEE International Conference on Circuits and Systems, vol. 2, pp. 271-274, Sep. 1998.

[2] S. H. Lewis and P. R. Gray, “A pipelined 5 Msamples 9-b analog-todigital converter,” IEEE J. Solid-state Circuits, vol. SC-22, pp. 954-961, Dec. 1987.

[3] Y.-M. Lin, B Kim, and P. R. Gray, “A 13 b 2.5 MHz self-calibrated pipelined A/D converter in 3 um CMOS,” IEEE J. Solid-state Circuits. vol. 26, pp. 628-636, Apr. 1991.

[4] P. C. Yu and H. S. Lee “2.5 v , 12 bit, 5 M-Sample/s pipeline CMOS ADC,”, IEEE J. Solid-State Circuits, vol. 31, pp. 18541861, Dec. 1996.

[5] A. Abo and P. Gray, “A 1.5 V, 10-bit, 14.3-MS/s CMOS pipeline analogto- digital converter,” IEEE J. Solid-State Circuits, vol. 34, pp. 599605, May 1999.

[6] P. Y. Wu, V. S. Cheung, and H. C. Luong, “A 1-V 100-MS/s 8-bit CMOS switched-opamp pipelined ADC using loading-free architecture,”IEEE J. Solid State Circuits, vol. 42, no. 4, pp. 730738, Apr.2007.

[7] S. Ryu, B. Song, and K. Bacrania, “A 10-bit 50-MS/s pipelined ADC with opamp current reuse,” IEEE J. Solid State Circuits, vol. 42, no. 3, pp. 475485, Mar. 2007.

[8] Chandrashekar, K.; Bakkaloglu, B., “A 10 b 50 MS/s Opamp-Sharing Pipeline A/D With Current-Reuse OTAs,” Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , vol.19, no.9, pp.1610-1616, Sept. 2011.

[9] Jipeng Li; Un-Ku Moon, “A 1.8-V 67-mW 10-bit 100-MS/s pipelined ADC using time-shifted CDS technique,” Solid-State Circuits, IEEE Journal of , vol.39, no.9, pp. 1468- 1476, Sept. 2004.

[10] H.Yu, S.W. Chin, and B. C.Wong, “A 12 b 50MSPS 34mW pipelined ADC,”in Proc. IEEE Custom Integr. Circuits Conf., pp. 297300, Aug. 2008.

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Table I: Summary of proposed A/D and prior work

References	**[8]**	**[9]**	**Proposed work**
Supply voltage	1.8 V	1.8 V	1.8 V
Technology	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS
Resolution	10 bit	10 bit	10 bit
Conversion rate	50 MS/s	100 MS/s	80 MS/s
Power dissipation	9.2 mW	67 mW	30 mW
DNL	±0.4	0.8 LSB	-0.5/0.14 LSB
INL	±0.7	1.6 LSB	-0.43/0.4 LSB
SNR SNDR SFDR	58.6 dB 58 dB 74.0 dB	- 54 dB -	60 dB 59 dB 68 dB