Plasma-Wave Enhanced THz-Performance of a Nanometer Side-Gated Transistor

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Abstract – By using a two-dimensional-three-dimensional (2D-3D) combined ensemble Monte Carlo (EMC) model, the performance of a nanometer side-gated transistor is studied at terahertz (THz) region. The transistor is based on a GaN/AlGaN heterostructure at whose hetero-interface a two-dimensional electron gas (2DEG) is formed. And the side-gate of the transistor is intentionally designed as an insulating trench with a 2DEG area in the center. Simulation results reveal that at low working frequency the performances of the transistor are almost frequency independent. However when the working frequency reaches THz region, obvious enhancements of the performances have been observed. The enhancements are accompanied by two peaks respectively at the frequency of about 4 THz and 6 THz. As such, the frequency-dependent performances become frequency nonmonotonic. Further analysis shows that the performance enhancements can be attributed to the excitations of 2D plasma waves in the side-gate which including a 2DEG area in its center.

Keywords – Monte Carlo, 2D Plasma Wave, Nanometer, Side-Gated Transistor, THz.

I. INTRODUCTION

Benefiting from miniaturization of semiconductor devices, a single silicon chip is now able to contain more than a billion transistors and operate at frequencies higher than GHz. Moreover, the operation frequency can be further increased by utilizing a planar architecture. In planar devices, electrodes are connected side by side to the active semiconductor layer rather than placed on top of each other, as in conventional multilayered vertical-structured devices. As such, very low parasitic capacitances are obtainable, leading to very high operating speeds. Planar devices based on 2DEGs in semiconductor heterostructures had been demonstrated to operate at least tens of GHz [1-3]. In particular, self-switching diodes (SSDs) had been shown to not only possess zero threshold voltages, but also be able to work as THz detectors. At room temperature they can operate with a speed up to 1.5 THz [4] and at a temperature of 150 K up to 2.5 THz [5].

Apart from resulting in higher frequency operations, the planar architecture also leads to some extra mechanisms. It had been shown that when the thickness of the conducting layer was lower than 10 nm, 2D ‘plasmonic noise’ was dominant, so that geometrical dependence of noise characteristics emerges [6]. Moreover it had been proved that in a nanometer field-effect transistor (FET) with asymmetric conditions, 2D plasma waves could be excited simply by a DC current [7]. This has wake up a widely interesting in studying of nanometer FETs as THz sources and detectors, resulting in rich achievements [8-13].

The physics of plasma wave based collective electron transport is much difference from conventional individual (uncorrelated) electron transport. However, the studies so far are mostly limited to FET structures. As such, based on our recently developed 2D-3D combined EMC model [14], we will focus on studying the effect of the 2D plasma waves on improving the THz performances of a nanometer side-gated transistor in this work. The paper is structured as follows. In Sec. 2, the structure of the transistor is firstly introduced and then the 2D-3D combined EMC model is concisely described. In Sec. 3, the frequency-dependent performances of the transistor are studied and the plasma related features are analyzed in detail. In Sec. 4, the conclusions of this work are summarized.

II. DEVICE STRUCTURE AND EMC MODEL

Figs. 1(a) and 1(b) show schematically the top view and cross section of a nanometer side-gated transistor. The transistor is based on a GaN/AlGaN heterostructure, where a 2DEG is formed at the GaN/AlGaN hetero-interface with a carrier concentration of 8.0×10^{12} cm^{-2} [15]. The two insulating trenches (gray areas in Fig. 1 (a)) are created by

Fig.1. Schematic top view (a) and side view (b) of the simulated side-gated transistor (not to scale). The grey areas and the white area in the top view represent insulating trenches and the 2DEG, respectively. A GaN/AlGaN interface is 30 nm below the device surface at which a 2DEG forms. In the simulations, all the insulating trenches are assumed to have vertical sidewalls and pass through the entire GaN/AlGaN heterostructure.
etching through the 2DEG layer. As such, electrons have to pass the narrow channel, between the two trenches, in order to conduct a current from the source to the drain. Obviously, the source-drain current can be controlled by the side-gate, which is intentionally designed as an insulating trench with a 2DEG area in the center as shown in Fig. 1 (a).

A 2D-3D combined EMC model based on a semi-classical 2D EMC method self-consistently coupled with 3D Poisson equations is used in this work. This combined model is developed from our entirely 2D model, which has been successfully used in earlier work [16-17]. It is noteworthy that a fully 3D EMC model has been developed to study three-terminal T-branch junctions (TBJs) with a top gate terminal [18-19]. In spite of minimizing the need for parameter fitting and including the effect of electron transfers from channel to other layers, the 3D model leads to almost the same results as those obtained from an entirely 2D model for GaAs based devices [20]. There are two reasons leading to the above agreement between entirely 2D model and 3D model. One is because that the operating properties of TBJs are mainly determined by the 2DEG layer which can be well described in an entirely 2D model. The other is because that an artificially-introduced side gate in the 2DEG layer can serve the function of TBJs’ top gate. If the top gate could not be modeled as a side gate, at least a 2D-3D combined model is needed.

Similar to an entirely 2D model, electrons in the combined model are assumed to be all confined within the 2DEG layer. This means that the effect of electron transfers, from channel to other layers, is ignored. As such 2D EMC method is enough to depict the micro behaviors of electrons in devices. The main advance of the combined model lies on upgrading the 2D Poisson solver in the entirely 2D model to a 3D Poisson solver. As such, electric field couplings beyond the 2DEG layer which lead to the appearance of 2D plasma waves can be properly included. In order to sufficiently include the 3D electric-field couplings, Poisson equations should be solved in a domain beyond the device’s realistic structure. As shown in Fig. 1 (b), the GaN substrate and a region (Air) above the device surface, both with height of 1 , were included during simulations. Insulating trenches were assumed to have vertical sidewalls. Moreover, the depth of all the insulating trenches was assumed to be 1030 nm. This uniform-depth treatment can avoid the trench-depth effect [14]. Dielectric constant used in the simulations for Air, AlGaN and GaN was 1, 8.5 and 8.9, respectively. For convenience, the influence of surface states at semiconductor-air interface was included by a simple constant charge model with negative charge density, \( N_s = 0.8 \times 10^{12} \text{ cm}^{-2} \) [21]. Of course, the use of advanced surface charge model, such as self-consistent charge model, would result in more accurate results, but it is time consumed and makes no qualitative difference [22].

Fig. 2. Current-voltage characteristics of the nanometer side-gated transistor, shown in Fig. 1, under different gate voltage \( V_G = -4.0 \text{ V}, 0.0 \text{ V}, 4.0 \text{ V}, 8.0 \text{ V}, 12.0 \text{ V} \).

The steady properties of the nanometer side-gated transistors shown in Fig. 1 are firstly studied. During the simulations, the source terminals of the nanometer side-gated transistors is grounded. To insure a steady state, the transistor is simulated with a sufficiently long time (tens of ps) under constant conditions. The current through the nano-channel is monitored and recorded when it no longer changes with time (i.e. slightly fluctuating around a fixed value). By averaging the recorded current, the drain current can be obtained.

Shown in Fig. 2 are the relationships between drain current and voltage when different gate voltage are applied. One can find that at low drain bias the current-voltage characteristics are almost linear. And with the increase of drain voltage, the nonlinearity of the current-voltage characteristics increase. When the gate voltage is larger than 9.0 V, the drain current of the nanometer side-gated transistor is almost unchanged with the drain voltage for all studied gate biases. Moreover, one can further find that the saturated drain currents also changes with gate bias. And the linear range is between zero voltage and 8.0 V. These results show that like the traditional transistors, the studied nanometer side-gated transistor has obvious field effect.

Fig. 3. Frequency-dependent current amplitude of the nanometer side-gated transistor shown in Fig. 1.
Fig. 3 shows the frequency-dependent performances of the nanometer side-gated transistor shown in Fig. 1. During simulations, the source is also grounded and the drain was biased with DC voltage of 15.0 V, which is just at the center of the saturated range. To insure linear performances, the gate was biased with DC voltage of 4.0 V, which is at the center of the linear range. Then a sinusoidal signal with amplitude of 1.0 V was further added and the AC current through the nano-channel was recorded. Fig. 3 tell us that the current amplitude at 0.1 THz is about 5.5 μA. One can also find from Fig. 2 that for fixed drain bias of 15.0 V, the current difference between gate bias of 0.0 V and 8.0 V is about 44μA. These result show a coincidence between steady performances and low frequency AC performances. The AC performances of the transistor remains almost unchanged at frequencies lower than 1.0 THz, and then show obvious enhancement (i.e., the amplitude of current is larger than that predicted by the steady performances) when the frequency is higher than 1.0 THz. The current amplitude increases with frequency and reaches its first maximal value (about twice of those at low frequencies) at the frequency of about 4 THz. After that it dramatically reduces and then increases again to reach the second maximal value at the frequency of about 6 THz. However, this second maximum is not pronounced and its value even smaller than those at low frequencies. Then the current amplitude monotonically reduces and reaches its minimal value, near zero, at the frequency of about 10 THz.

Previous work shows that the high frequency performances of planar nano-devices can be strongly enhanced by 2D plasma waves [24]. As one can find from Fig. 1, the gate insulating trench possesses a 2DEG layer in its center, forming a resonance for selecting 2D plasma waves. As such, 2D plasma waves should play an important role in the high frequency performances of the studied transistor, especially when AC signals are inputted through the gate terminal. In order to find out the relationship between above performance enhancements and 2D plasma wave resonances, the properties of 2D plasma waves in the gate insulating trench will analyze in detail. The dispersion relations of 2D plasma waves are given by [6],

\[ f = \frac{1}{2\pi} \sqrt{\frac{e^2 n^{2D} k}{2m_0 m_\text{eff} \varepsilon_\text{eff}}} \]  

(1)

Where \( f \) and \( k \) are the frequency and wave vector, respectively, \( e \) is the electron charge, \( n^{2D} = 8 \times 10^{12} \text{cm}^{-2} \) is the 2D carrier concentration, \( m_0 \) and \( m \) are the free and effective electron masses, \( \varepsilon_\text{eff} \) is the vacuum dielectric permittivity, and \( \varepsilon_\text{eff} \) is the effective dielectric constant [25]:

\[ \varepsilon_\text{eff} = \frac{1}{2} \left[ \varepsilon_1 + \varepsilon_2 \frac{1 + \varepsilon_1 \tanh(kd)}{\varepsilon_1 + \tanh(kd)} \right] \]  

(2)

In our case, \( \varepsilon_1 = 8.5 \) is the dielectric constant of AlGaN, \( \varepsilon_2 = 8.9 \) is the dielectric constant of GaN and \( d = 30 \text{nm} \) is the thickness of AlGaN layer. The standing wave conditions in a closed resonance are known as,

\[ k = \frac{n \pi}{L} \]  

(3)

Where \( n = 1, 2, \ldots \) and \( L = 400 \text{nm} \) is the length of reservoirs. Substituting (2) and (3) into (1) and using the parameters provided above, one can obtain that the frequency of standing waves is 4.5 THz and 6.4 THz for \( n = 1 \) and 2, respectively. Since damping effects (e.g. phonon scatterings) are not included in (1), analytic results obtained from (1)-(3) are expected to be higher than those simulation ones that including all the damping effects. By making a comparison, one can find that each analytically-obtained frequency is just a little higher than the frequency of the maximal value of current amplitude shown in Fig. 3, respectively. This tell us that the enhancement of transistor performances at THz region is because of the excitations of 2D plasma waves. And the forming of standing plasma waves in the resonance of the gate insulating trench attributes to the performance peaks (maximal values of current amplitude) shown in Fig. 3.

**IV. CONCLUSION**

In this paper, we have employed a combined 2D-3D EMIC model to analyse the steady and high frequency performances of a GaN-based planar nanometer transistor under different conditions. The side-gate of the studied transistor is intentionally designed as an insulating trench with a 2DEG area in its center. We observed that the studied transistor possesses obvious field effects. And at low working frequency the AC performances of the transistor are almost frequency independent and coincident with steady performances. Moreover, the performance of the device at frequencies higher than 1.0 THz is strongly enhanced by 2D plasma waves. The resonances of the 2D plasma waves with the designed gate structure result in two performance peaks at frequencies of about 4 THz and 6 THz, respectively. Such a resonant property may enable not only higher ability of controlling current through the nano-channel but also a degree of frequency selectivity, which may have useful implications in RF circuits or THz systems.

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**REFERENCES**


