Capacitance Measurement Methods for Integrated Sensor Applications

Alireza Hassanzadeh, Robert G. Lindquist

Abstract – In this paper different measurement methods that have been used for integrated capacitance measurement are reviewed and their advantage and disadvantages are discussed. For the designers of high accuracy on chip integrated circuits for capacitive sensors, it is important to know which method will provide the best approach for high accuracy, small chip area and power consumption especially for array sensors. These methods include on chip capacitive sensor and transducer measurement techniques that have been implemented for low value capacitance evaluations using CMOS technology. After the best structure is known the designer can optimize the chip for specific application. Voltage mode and current mode, linear and switched mode techniques are reviewed and a useful comparison table comparing all figures of merit including accuracy, range of measurement, chip area, speed and complexity is provided. The provided comparison table can be used as a reference for analog designers in the design of high accuracy integrated capacitive sensor interface.

Keywords – CMOS Interface Circuit, Capacitive Sensor, Sensor Integration, Capacitance Measurement, System on a Chip.

I. INTRODUCTION

Capacitive measurement techniques have been developed through years and many techniques have been presented even in textbooks [1-3]. Recent advances in MEMS and integration of sensor devices with interface circuitry has demanded for integrated measurement methods that can push the accuracy and resolution limits of the measurement. MEMS accelerometer, capacitive tomography, particle detectors, lab-on-chip systems are some examples of these systems. Because of stray and cable capacitances it is hard to measure capacitance in the range of Atto and Femto Farads on discrete systems. Integration reduces parasitic capacitance and increases system resolution. Some high accuracy accelerometers would not be possible without integrated circuit implementation. CMOS technology is an inexpensive and promising technology for integrated sensor applications. Most interface circuit designs have been developed using voltage mode signal processing and some used current mode implementations. Current mode signal processing does not need high voltage swing and can be used for low voltage applications. Accuracy of current mirrors limits these kinds of circuit applications.

Previous work in reference [1] introduces low power capacitive sensor interface design using CMOS circuits that mostly focus on switched capacitor and sigma-delta technique implementation and does not review all reported techniques for capacitance measurement. Reference [2] reviews different capacitance electrode for sensor configuration and basic principles of capacitance measurement techniques. Impedance matching and some applications are discussed but it does not focus on CMOS implementation. Recently published journal paper in [3] has reviewed CMOS capacitive sensors for lab-on-chip applications, and its main focus is on the general system design including electrodes and micro fluidic implementation problems in CMOS technology. It does not provide a comparison of methods and the circuit part is focused on CBCM (Charge Based Capacitance Measurement) technique and not all previously reported methods.

In this paper different capacitance measurement techniques for integrated CMOS implementation are reviewed and their limitations and resolution are discussed. A useful comparison table is provided that gives a general view for circuit designers to choose from different techniques based on the required accuracy and complexity. This paper is arranged as follows. First different CMOS integrated voltage and current mode techniques and their principle of operation are discussed. A comparison of measurement merits is provided afterward. The conclusion remarks are at the end.

II. INTEGRATED CAPACITANCE MEASUREMENT TECHNIQUES

In this section different CMOS circuits reported for capacitive sensor interface are reviewed. The most common and easy to design method for implementing capacitance measurement is charge and discharge method. The voltage developed across a capacitance is proportional to the charging current. The larger the capacitor the longer it takes to charge with constant current. Since the time can easily be measured using a simple counter, digital output is easily available. This method actually is a capacitance to time duration converter. By using a voltage comparator, it is possible to convert the voltage ramp into a pulse width. The pulse width is proportional to capacitance value. This method has been used for array of DNA sensor integrated system [4]. The block diagram of the system is shown in figure 1.

A reference current, \( I_{REF} \) is used to charge and discharge the sensor capacitor using CMOS switches. The interdigitated capacitive sensor is between \( V_A \) and \( V_B \) and the voltage across that is compared with \( V_{REF} \) using a differential comparator. As shown in the waveforms, the output of the comparator is a pulse with period \( T \), proportional to the time it takes to charge and discharge the capacitor and therefore the capacitance value. Producing an accurate reference current source and a good comparator usually limit the accuracy of this method. Furthermore, parallel stray capacitances are not canceled.
using this method. The range of reported measurement is from 330pF to 10nF with 1% error. The advantage of this method is its simplicity and direct digital output besides small chip area. It has been used for an array of 128 DNA sensors.

For smaller capacitance range, such as capacitance of interconnection wires in an integrated circuits, a method called Charge Based Capacitance Measurement (CBCM) has been introduced [5]. Two identical CMOS inverters have been used to provide a differential measurement. One inverter is dummy and the output of the other inverter is connected to the unknown capacitor between two wires A and B, as shown in figure 2. These two inverters are excited using pulses Vp and Vn, in a way that PMOS and NMOS transistors are not ON at the same time. Therefore, the capacitance at the output node of the inverters is charged to the supply voltage via PMOS transistor and discharged via NMOS transistor alternatively. The average current pulled from the supply voltage (I1, I2) is proportional to the capacitance value at the inverter output node. By using an analog current meter, it is possible to measure the average current difference that is proportional to the unknown capacitance. Since differential method has been used, parasitic capacitances are canceled out and the charge difference is only proportional to the load capacitance at node P. This method has also been used for lab-on-chip applications for array of sensors [6]. Figure 2 shows the basic schematic of CBCM method.

External analog current meters can be used for the difference current measurement. In contrast, current mirrors can be used to produce difference current on chip, which usually reduces the accuracy, because of mismatch problems. Range of measurement of this method has been reported as 20fF with 10aF resolutions. The disadvantage of this method is limited range of measurement and using current mirrors that usually do not provide good matching [7-11].

Using the idea of differential measurement and charge transfer, a method has been developed that is capable of doing differential, absolute and ratio metric capacitance measurement. The block diagram of this method has been shown in figure 3. Using analog switches and four arm capacitors C1 to C4, unknown capacitor can be evaluated. In the first phase, S1 and S4 are closed and the capacitors are charged to the supply voltage. In the second phase, S2 and S4 are closed and capacitors are connected to the source of the four transistors. Because of low impedance of the source, parasitic capacitances will be cancelled out. The charge difference between these capacitors are transferred and sampled on C5 to C8 capacitors. The offset inputs can be used for offset adjustment or to provide negative feedback from OTA. This method has a 66dB dynamic range and minimum sensitivity to CMOS process variation. Sensitivity of this work has been reported to be 1.56mV/fF with maximum of 640fF measurement range [12].

Adding switches to circuit usually adds more problems such as charge injection and offsets. To avoid charge injection some all-analog methods have been developed. Many linear charge amplifiers have been reported in the literature for capacitance measurement. These linear circuits normally need analog offset and gain adjustments [29]. Synchronous detection or lock-in detection technique uses all continuous time signal processing to measure the capacitor value. In this method capacitance value is modulated with a known signal, and after amplification using synchronous demodulation the original signal will be retrieved. In this method, low frequency noise, DC offset and other off-band signals will be modulated to higher frequencies.
The original signal will be demodulated and restored using a low pass filter at the output. Although demodulator adds some complexity to the circuit such as non-linearity and offset compensation, still has very high resolution. Because this method does not use switches, charge injection will not cause problem. Very high sensitivities have been reported using this method. Figure 4 shows block diagram of such a system [13].

A square wave signal is applied to the capacitors and the output signal is amplified using a differential charge amplifier. Input and output common mode feedback have been used to stabilize DC biasing. After amplifier, a demodulator and low pass filter will provide the DC output signal, which is proportional to the capacitance difference. Sensitivity of 26.5aF in 0.44pF range with 81dB dynamic range has been reported for this method [13]. This method also has been used in reference [14] using BiCMOS process that utilizes analog multiplier instead of switched demodulators to achieve higher sensitivity of the measurement. Similar techniques have been used in other papers [15-18].

A group of techniques have been developed known as current mode circuits that process the signal in current instead of voltage. Block diagram of a simple current mode method for capacitance measurement is shown in figure 5. A current source is used to excite two capacitors and the output current is differentially amplified using differential current amplifier.

Current mode signal processing does not need large voltage swing therefore it can be used for low voltage applications. A current mode implementation of sensor capacitance change measurement is shown in figure 6. Differential capacitors are excited using a triangular waveform and instead of voltage amplifier current amplifier has been used to amplify the sensor signal. All offset canceling and other signal processing are done in current mode [18]. The current output of the CA is added to the current $\Delta I_B$ and $I_D$ to charge capacitor C. The triangular excitation waveform is synchronized with the clock signal. The switches SA1 and SA2 change the polarity of the signals to charge and discharge capacitor C in each half cycle of the clock period. The current $\Delta I_B$ is larger than $I_D + \max \left| I_{CA} \right|$ to make the circuit operate properly. The waveforms of the circuit operation are shown in figure 6. In the first half cycle of the clock period, the capacitor C is charged and in the second half of the clock period the switches SA1 and SA2 change polarity and the capacitor starts to discharge. As the capacitor voltage C becomes negative the comparator output changes state. The output pulse width is proportional to the capacitance difference.

Another current mode dual slope method implemented in BiCMOS technology is shown in figure 7. Three integrators have been implemented using OTAs. A reference capacitance $C_R$ on the feedback loop of G1 is charged using a reference current $I_{RMP}$. The unknown capacitance $C_X$ is in the feedback loop of G2 integrator. The feedback loop of G3 makes $V_{RMP} = V_X$ and as a result $I_1 = I_2$. The current $I_{SH}$ is a reference current that is subtracted from $I_2$ and the difference current is used to charge feedback capacitance $C_I$, on G4 OTA. After integrating phase, the input current is disconnected using S3 and discharge current $I_{DIS}$ via S4 discharges the integrating capacitor $C_I$. The output voltage of G3 goes to the comparator that produces a pulse with duration proportional to the unknown capacitance value. Range of reported measurement is 0.88-1.2pF [20]. The parasitic capacitances of the sensor are compensated using low impedance nodes of G2 OTA.

Switched capacitor circuits have proved to be successful candidates for analog interface design, especially in CMOS technology [22-27]. One of the challenging problems in analog circuit design is implementing high resistor values for low frequency circuits, which can easily be overcome by switched capacitor techniques. In addition, high matching between the capacitors can be achieved on a CMOS die. Therefore, it is possible to build very accurate circuits using switched capacitor techniques. Many other analog circuit problems such as DC offset can easily be compensated using this technique. The correlated double sampling (CDS) or auto zero techniques provide offset cancellation. A series of circuits have been reported for capacitance measurement using switched capacitor techniques. The schematic of this technique is shown in figure 8.
The principle of operation is to integrate the charge difference between an unknown and a reference capacitor. The charge difference between these two capacitors is integrated on a feedback capacitor. The output voltage of the integrator is proportional to the capacitance difference. Sensor capacitors are $C_{sl}$ and reference capacitors are $C_{ref}$ that can be selected using analog switches for different ranges. In order to avoid capacitor saturation, a switch discharges the integrating capacitor frequently. Series dummy switches have been used to reduce charge injection. The second charge amplifier stage has been used for variable gain implementation using $\phi_3$-$\phi_6$ switches and $C_{sl2}$ capacitors. In addition, parallel parasitic capacitances are also canceled because of low impedance input of the OpAmp. By using switched capacitor techniques, there will be no need for high value resistors in a feedback loop to bias the amplifier. This resistor has effect on frequency response of the amplifier. Furthermore, DC offset cancellation can be achieved easily using auto zero techniques. Besides these advantages switched capacitor circuit can be followed by a sigma-delta analog to digital converter that is not sensitive to process and does not need accurate components for high accuracy A/D conversion.

A more complete technique that uses differential technique and CDS for offset cancellation is shown in figure 9. This technique has been used for a micro gravity MEMS accelerometer. The measurement system uses a bridge configuration consisting of sensor and reference capacitors. The difference signal is amplified using a two phase switched capacitor charge amplifier that uses CDS capacitors for offset cancellation. Amplifier output signal is sampled on a sample and hold buffer to go to A/D converter. This method has been used for a high accuracy accelerometer in [28].

There are many other reported techniques in the literature for integrated capacitance measurement that are mostly derivative of the above-mentioned methods. In the next section these techniques are compared for different figures of merit.

### III. COMPARISON OF THE TECHNIQUES

Different techniques presented in this paper have their own advantages and disadvantages that make them suitable for specific application. Lock-in detection and CBCM techniques show the highest resolution in the reported papers and their resolution goes down into Femto and Atto Farad range. Switched capacitor, charge transfer, and current mode techniques stay next in the resolution ranking. For accuracy of measurement because switched capacitor technique provides many unique advantages like offset compensation and good matching properties, has provided highest accuracy in measurement techniques. Lock-in detection and CBCM and current mode techniques come afterwards. Charge discharge and switched capacitor also provide high dynamic range of measurement, especially if adjustable gain is provided. Form speed of measurement point of view, current mode, lock-in and CBCM techniques lead other measurement methods because of simplicity and mostly analog structures rather than switching methods. In general, analog techniques such as charge amplifier and lock-in detection will provide very high resolution and accuracy but there are difficulties from offset cancellation and large resistance implementation for low frequency applications. Switched capacitor techniques provide better control on offset and low frequency applications, but suffer from charge injection and switching problems. Table 1 summarizes some of the above-mentioned merits from high to low for the measurement techniques. This table has been sorted using information and accuracy values provided by the publishers referenced in this paper. Although, values are shown for each technique, these values do not mean that the technique cannot be used in other range of measurement. Table 2 provides chip area, complexity and type of output of these methods.
Table-1: Comparison of different capacitance measurement methods

<table>
<thead>
<tr>
<th>Resolution</th>
<th>Accuracy</th>
<th>Range</th>
<th>Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Lock-in (~0.1fF)</td>
<td>Charge Discharge</td>
<td>Current Mode Differential</td>
</tr>
<tr>
<td></td>
<td>Switched Cap.(0.01%)</td>
<td>(~100p-10fF)</td>
<td>(~500ns)</td>
</tr>
<tr>
<td>2</td>
<td>CBCM (~10aF)</td>
<td>Switched Cap.</td>
<td>CBCM (~10 s)</td>
</tr>
<tr>
<td></td>
<td>(~p-nF)</td>
<td>(~pF)</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Switched Cap. (~0.1fF)</td>
<td>Current Mode</td>
<td>Current Mode</td>
</tr>
<tr>
<td></td>
<td>CBCM (~0.5%)</td>
<td>Differential</td>
<td>Dual Slope</td>
</tr>
<tr>
<td>4</td>
<td>Charge Transfer (0.5fF)</td>
<td>Current Mode</td>
<td>Current Mode</td>
</tr>
<tr>
<td></td>
<td>Current Mode Dual Slope (~0.6%)</td>
<td>Mode Differential</td>
<td>Dual Slope</td>
</tr>
<tr>
<td>5</td>
<td>Current Mode Dual Slope (~0.9fF)</td>
<td>Charge Discharge</td>
<td>(~1%)</td>
</tr>
<tr>
<td></td>
<td>Current Mode Differential</td>
<td>(~1.2fF)</td>
<td>(~50 s)</td>
</tr>
<tr>
<td>6</td>
<td>Current Mode Differential</td>
<td>Charge Transfer</td>
<td>Switched Cap.</td>
</tr>
<tr>
<td></td>
<td>(~1fF)</td>
<td>(~0.8fF)</td>
<td>(~100 s-m)</td>
</tr>
<tr>
<td>7</td>
<td>Charge Discharge (~pF)</td>
<td>Current Mode</td>
<td>Charge Transfer</td>
</tr>
<tr>
<td></td>
<td>Current Mode Differential</td>
<td>(~2%)</td>
<td>(~200 s)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Method</th>
<th>Complexity</th>
<th>Area Used</th>
<th>Output Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lock-in Detection</td>
<td>Complex</td>
<td>Large</td>
<td>Analog</td>
</tr>
<tr>
<td>Switched Capacitor</td>
<td>Complex</td>
<td>Large</td>
<td>Analog/Digital</td>
</tr>
<tr>
<td>CBCM</td>
<td>Simple</td>
<td>Small</td>
<td>Analog</td>
</tr>
<tr>
<td>Charge Transfer</td>
<td>Complex</td>
<td>Large</td>
<td>Analog</td>
</tr>
<tr>
<td>Current Mode Dual Slope</td>
<td>Complex</td>
<td>Large</td>
<td>Digital</td>
</tr>
<tr>
<td>Current Mode Differential</td>
<td>Simple</td>
<td>Small</td>
<td>Analog/Digital</td>
</tr>
<tr>
<td>Charge Discharge</td>
<td>Simple</td>
<td>Small</td>
<td>Digital</td>
</tr>
</tbody>
</table>

Table 2: Complexity, chip area and output signal type of methods

IV. CONCLUSION

The growing area of on-chip capacitive sensor integration, demands for a good review paper that introduces different CMOS implementations and comparison of the methods for designers. In this paper different methods for integrated capacitance measurement were presented and their advantages and disadvantages were discussed. The comparison table provided will give a quick decision making aid for the range of measurement and accuracy of the techniques.

REFERENCES

[10] L. Vendrame, L.Bortesi, A.Bogliolo, “Accuracy and improvement of on chip charge based capacitance measurement”, University of Urbino Italy.
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